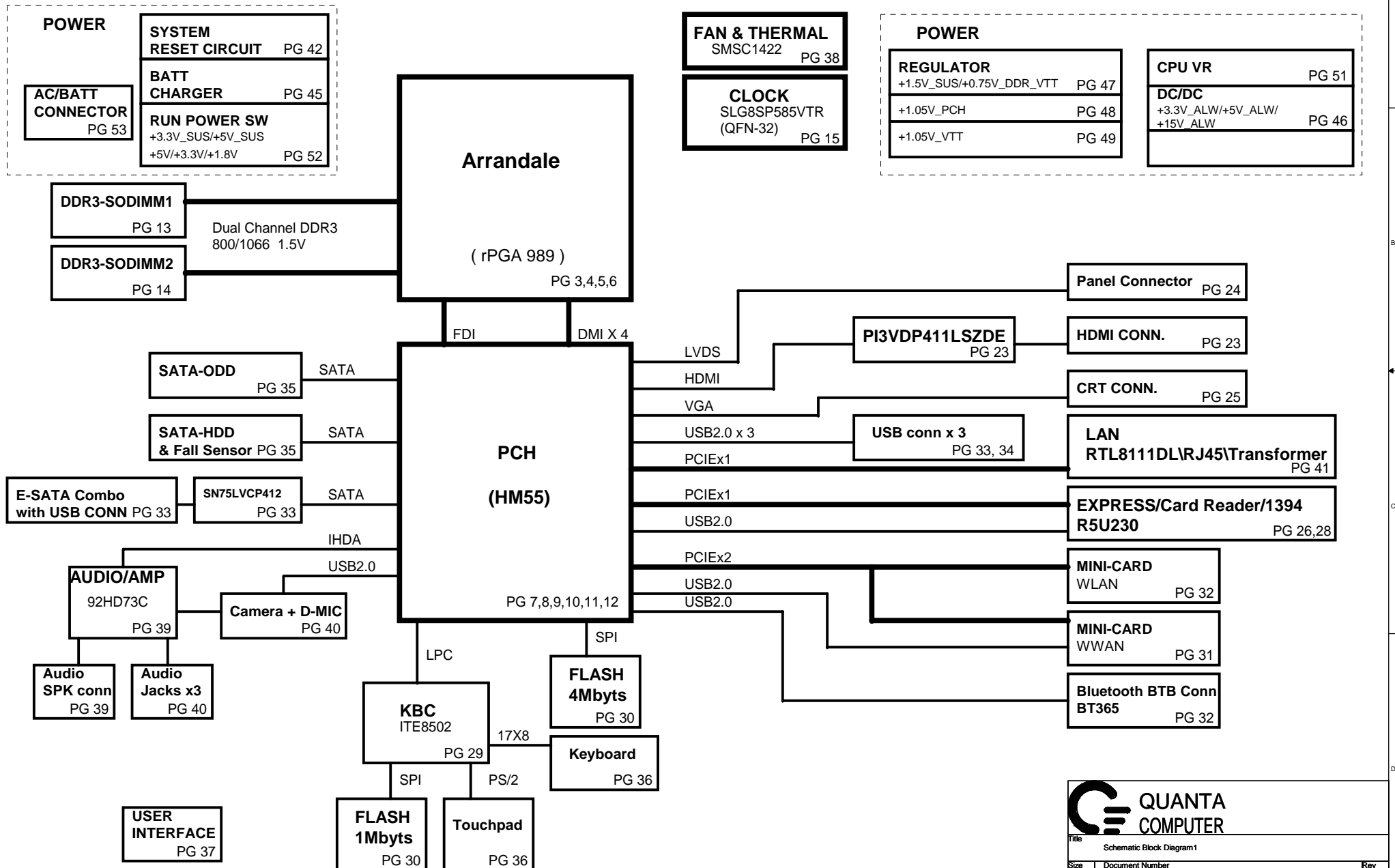


# FM9B HANKS Intel UMA

VER : 2B

PWA:

PWB:




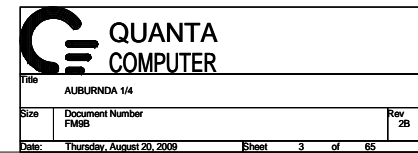
## Table of Contents

PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3-6	Clarksfield/Auburndale
7-12	PCH
13-14	DDRIII SO-DIMM(204P)
15	Clock Generator
16-22	BLANK PAGE
23	HDMI CONN
24	LCD CONN
25	CRT CONN
26	R5U230
27	BLANK PAGE
28	Express/CRard/1394
29	SIO (ITE8502)
30	FLASH / RTC
31	MINI-Card (WWAN)
32	MINI-Card (WLANWPAN)
33	Left USB/ESATA
34	Right USB
35	SATA (HDD & CD-ROM)
36	TP / KEYBOARD
37	SWITCH / LED
38	FAN / THERMAL
39	Azelia CODEC
40	AUDIO CONN
41	LAN(RTL8111DL/RJ-45)
42	System Reset Circuit
43	Blank Page
44	1.8V_RUN(RT9018/RT9024)
45	Charger (MAX8731)
46	3V/5V (TPS51427A)
47	1.5_DDR/0.75(TPS51116)
48	1.05V_PCH(TPS51218)
49	1.05_VTT(TPS51218)
50	GFX_VCORE (MAX17028)
51	CPU CORE(MAX17036)
52	Run Power Switch
53	DCin & Batt
54	PAD & SCREW
55	EMI CAP
56	SMBUS BLOCK
57	THERMAL MAP
58	Power Block Diagram
59	Power sequence Block
60	XDP

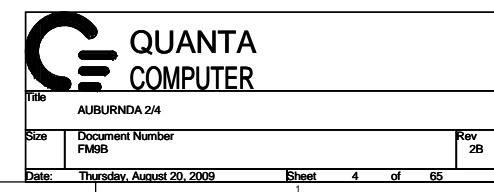
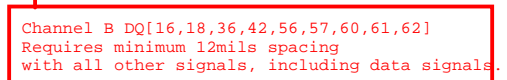
## Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	08,11,29,30	RTC		S0~S5
+5V_ALW2	+5V	37,46,52,53	LARGE POWER	MAIN POWER	S0~S5
+5V_ALW	+5V	13,33,44,46,47,48,49,50,51,52	LARGE POWER	ALW_ON	S0~S5
+3.3V_ALW	+3.3V	29,30,35,36,37,42,44,45,46,47,51,52,53	8051 POWER	3.3V_ALW_ON	S0~S5
+5V_SUS	+5V	11,33,34,37,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	07,08,09,10,11,13,14,19,24,28,29,37,41,42,44,48,49,50,52	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	03,05,13,14,47,50,52	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	13,14,47,52	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	11,18,24,25,35,36,38,39,40,51,52	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,7,8,9,10,11,13,14,15,17,24,25,26,28,29,30,31,32,33,35,37,38,39,40,41,42,46,51,52,60	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	05,11,44,52	SDVO POWER	RUN_ON	
+1.05V_VTT	+1.1V	03,05,10,11,49,60	CPU POWER	RUN_ON	
+1.5V_RUN	+1.5V	11,28,31,32,52	Express Card/Min Card	RUN_ON	
+5V_HDD	+5V	35	HDD Power	HDDC_EN	
+1.05V_PCH	+1.05V	08,09,11,15,48	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	05,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	24	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	35	MOD Power	MODC_EN	

GND PLANE	PAGE	DESCRIPTION
 GND	ALL	

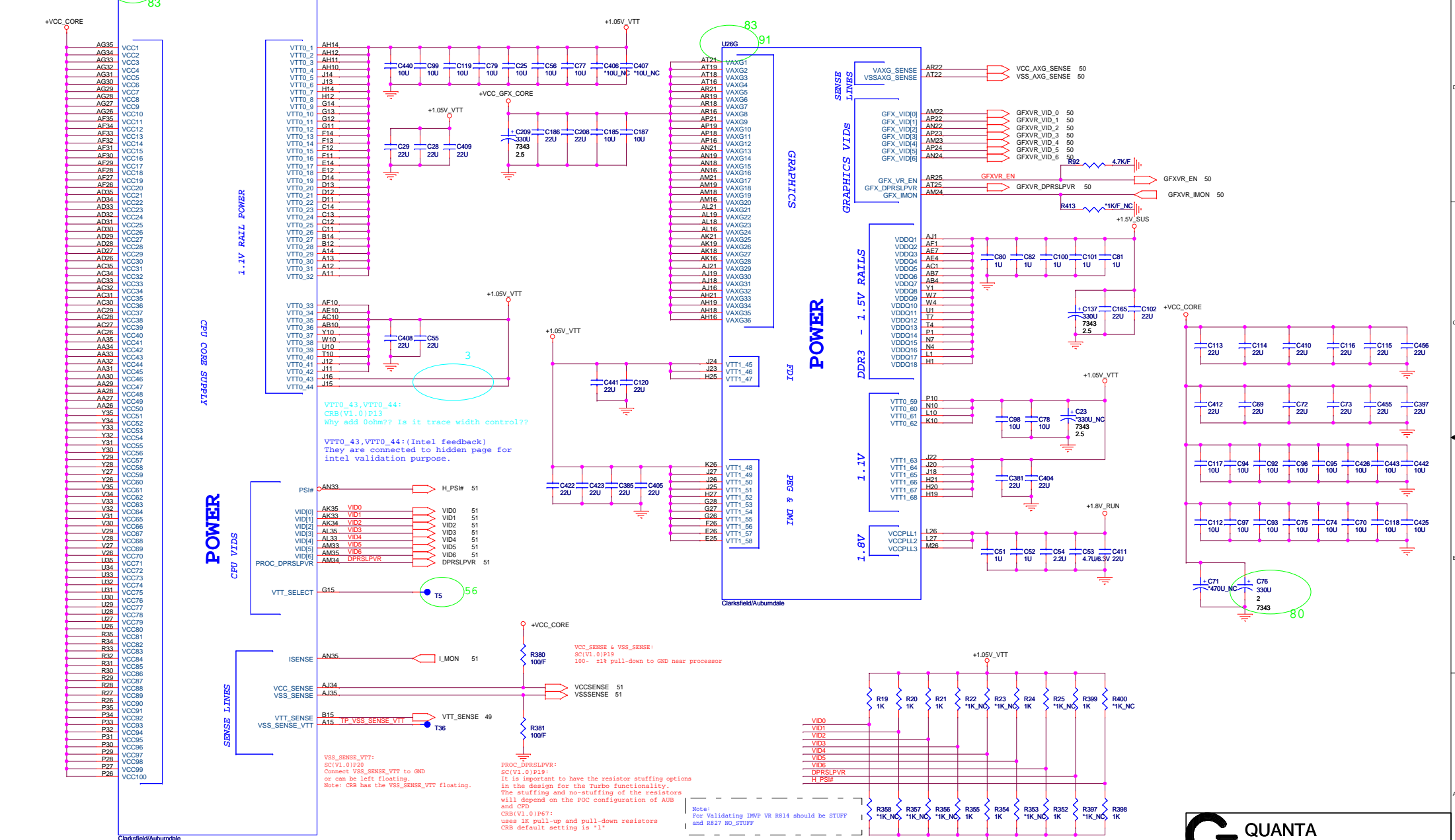


DR3 ) 83  
91 U26D



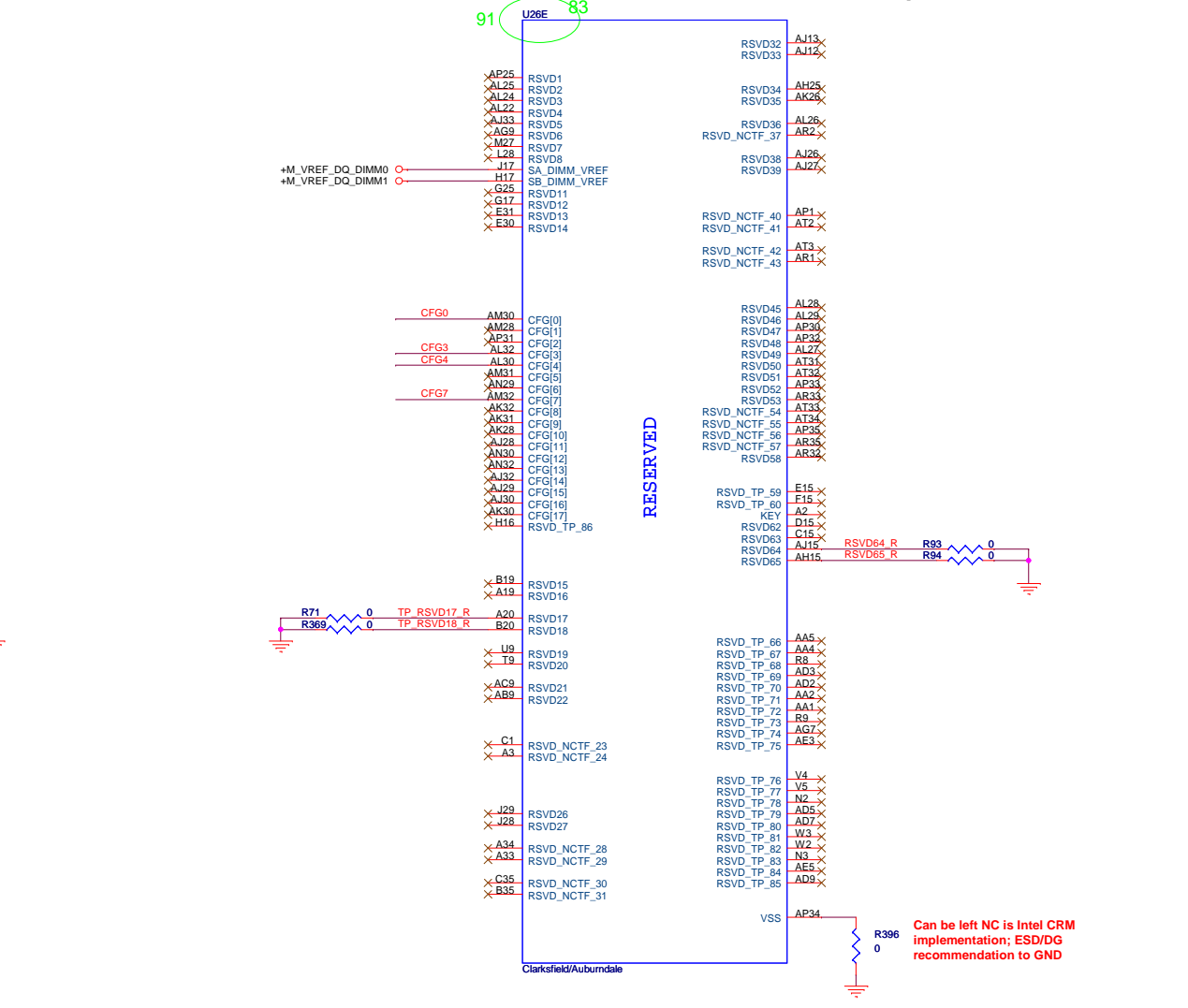
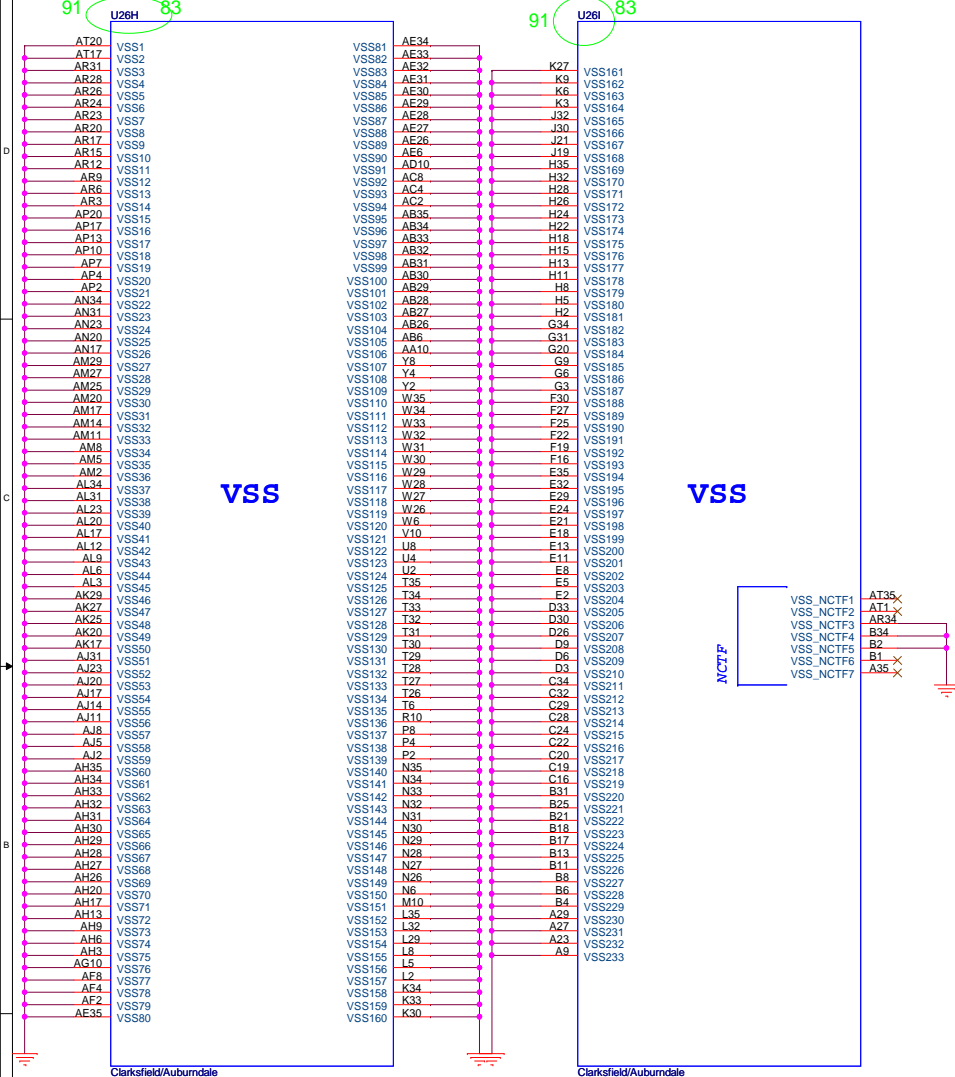
CPU Core Power

AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)

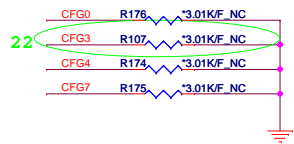


# AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

# AUBURNDALE/CLARKSFIELD PROCESSOR( RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



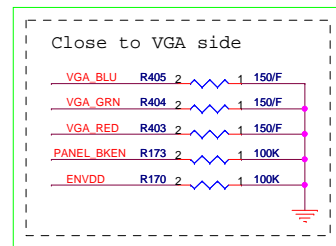
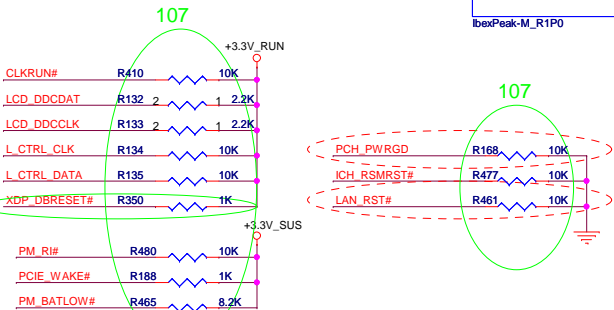
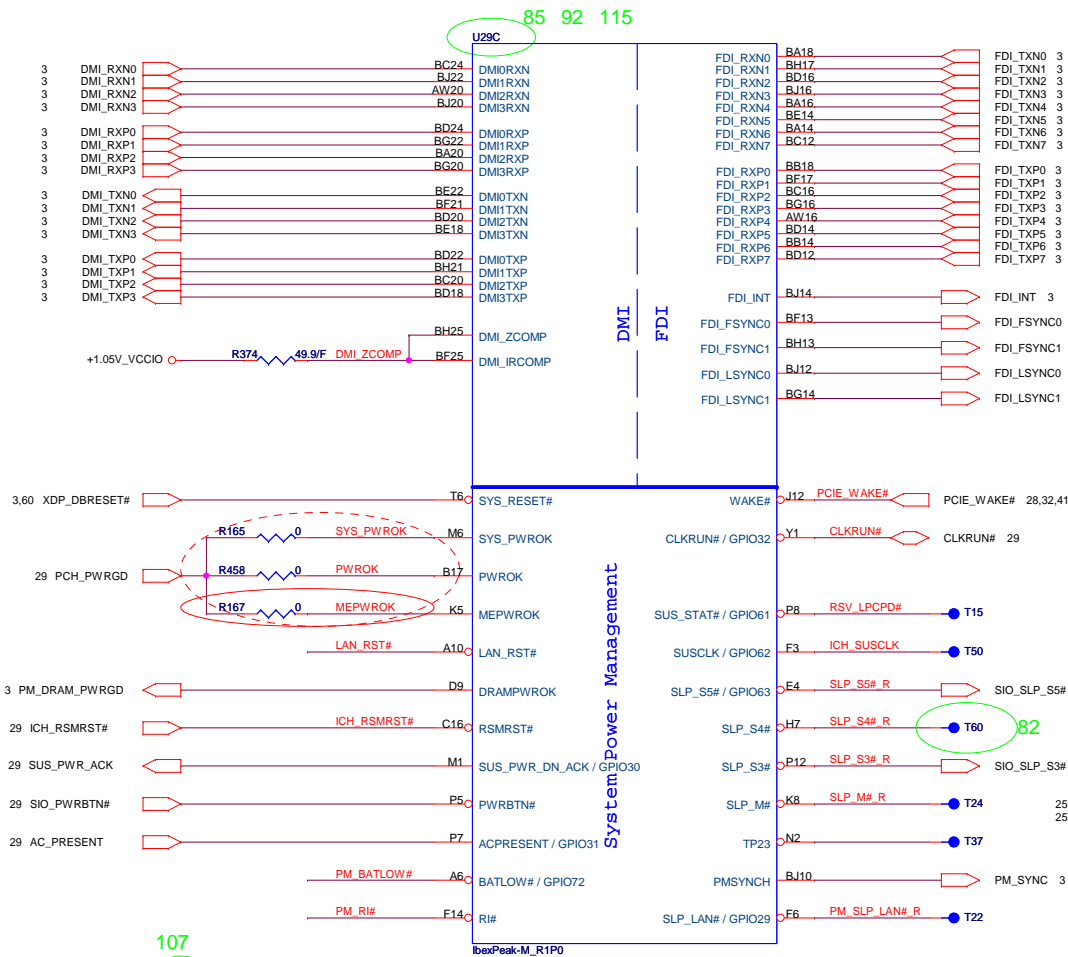
	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

QUANTA

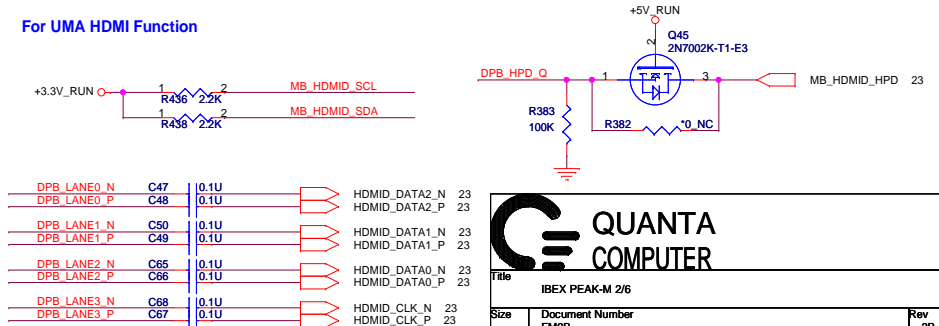
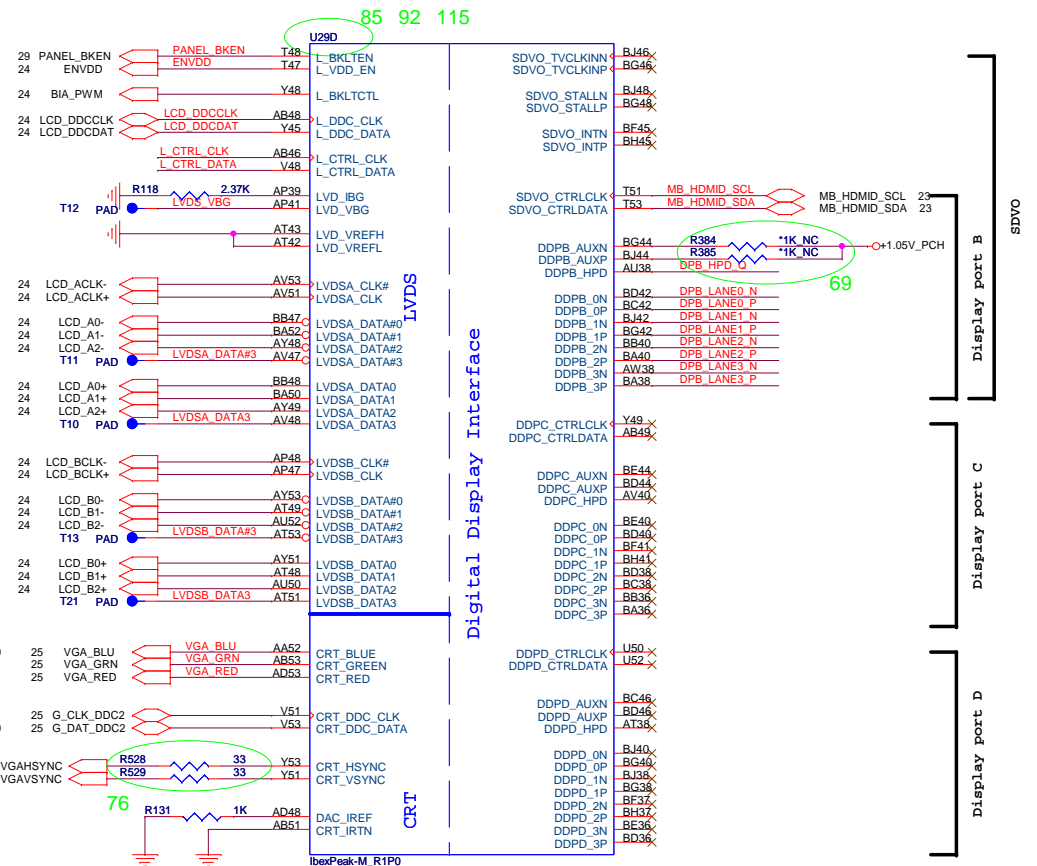
COMPUTER

Title AUBURND 4/4		
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## IBEX PEAK-M (DMI,FDI,GPIO)

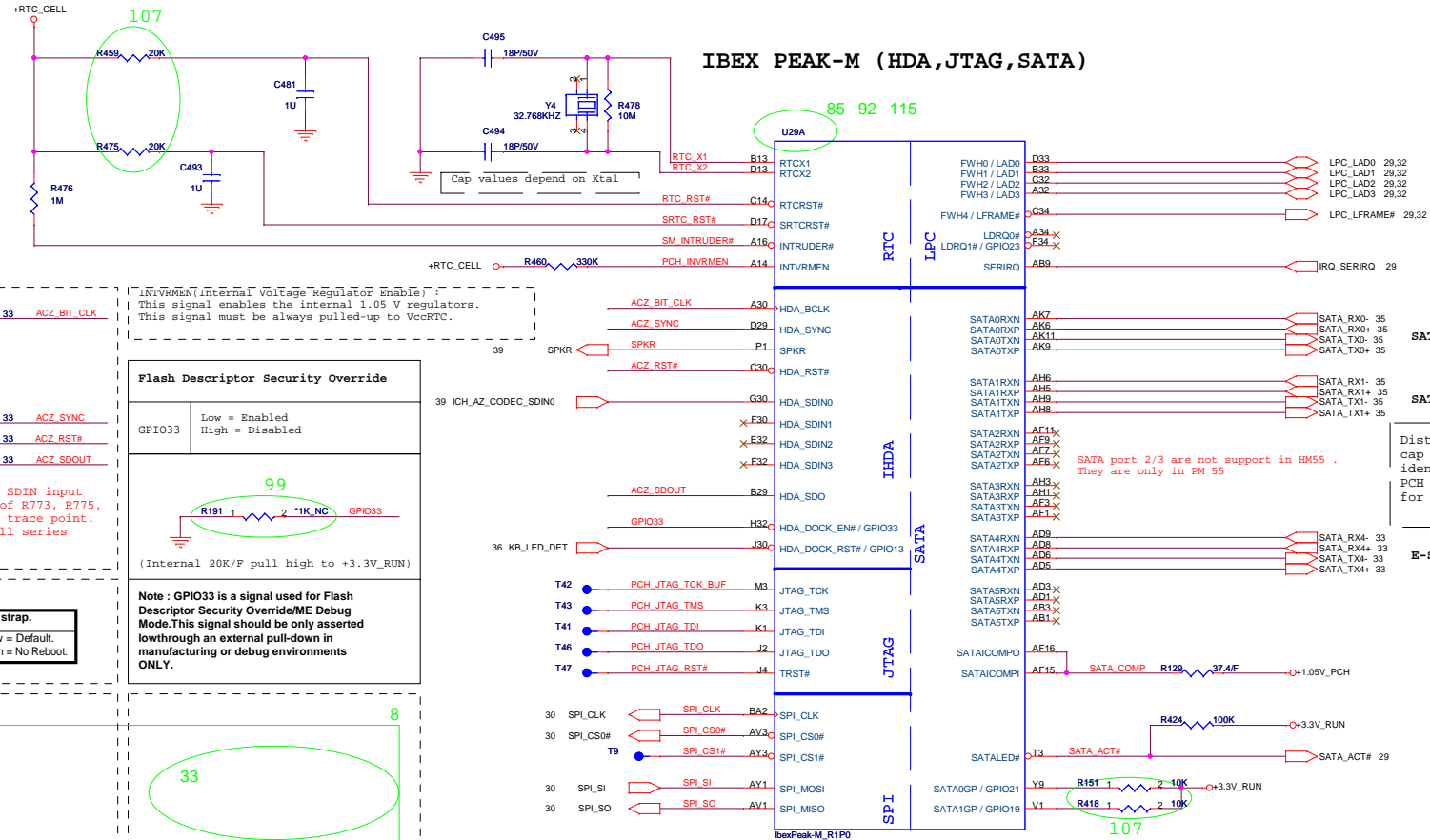


## IBEX PEAK-M (LVDS, DDI)





# IBEX PEAK-M (HDA,JTAG,SATA)



IBEX PEAK-M 1/6

Size	Document Number	Rev
	FM98	2B

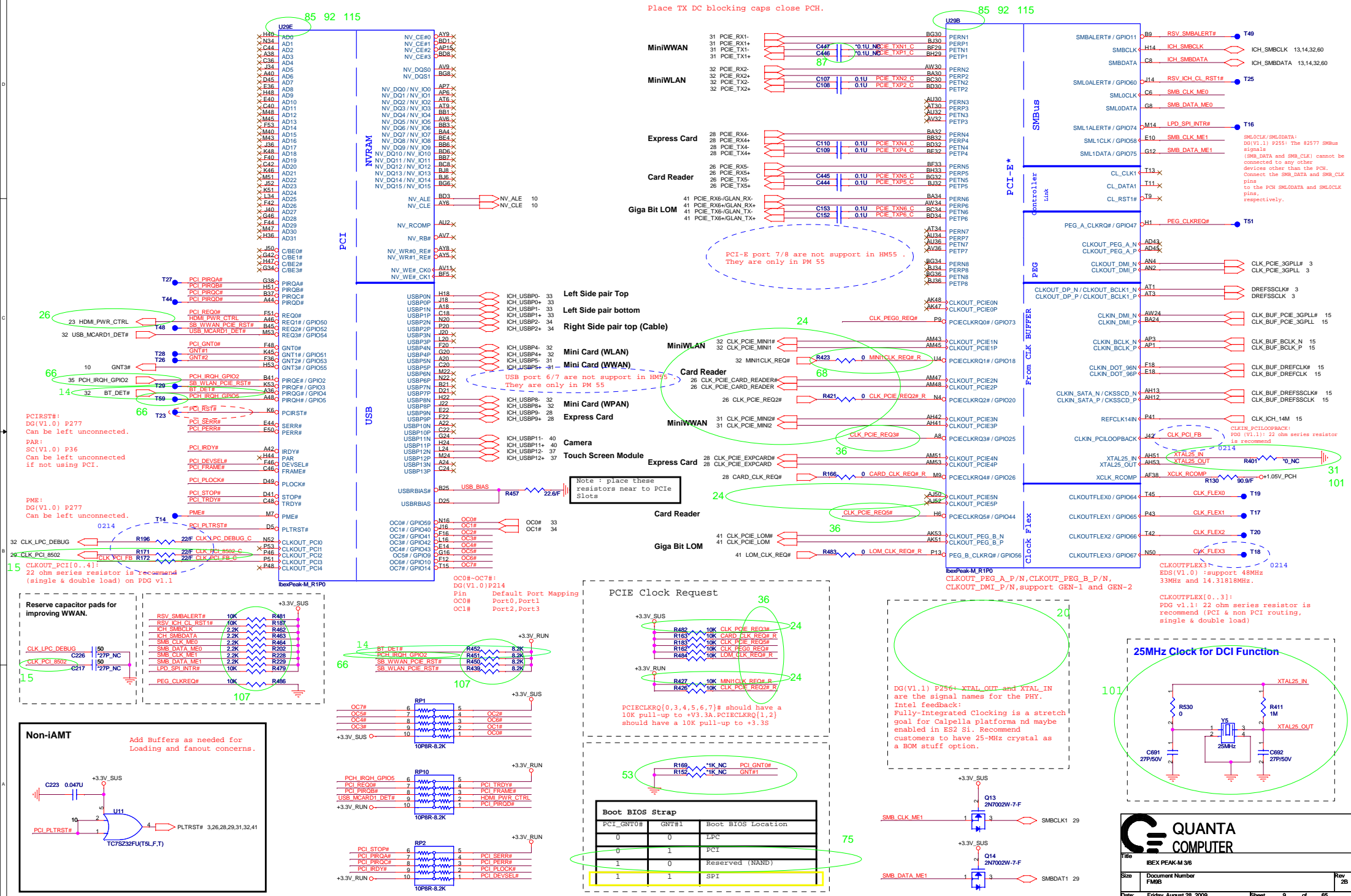
Date: Tuesday, September 01, 2009 Sheet 8 of 65



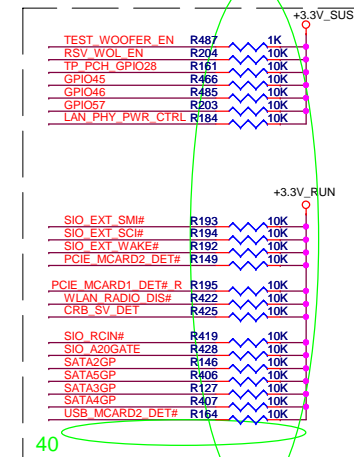
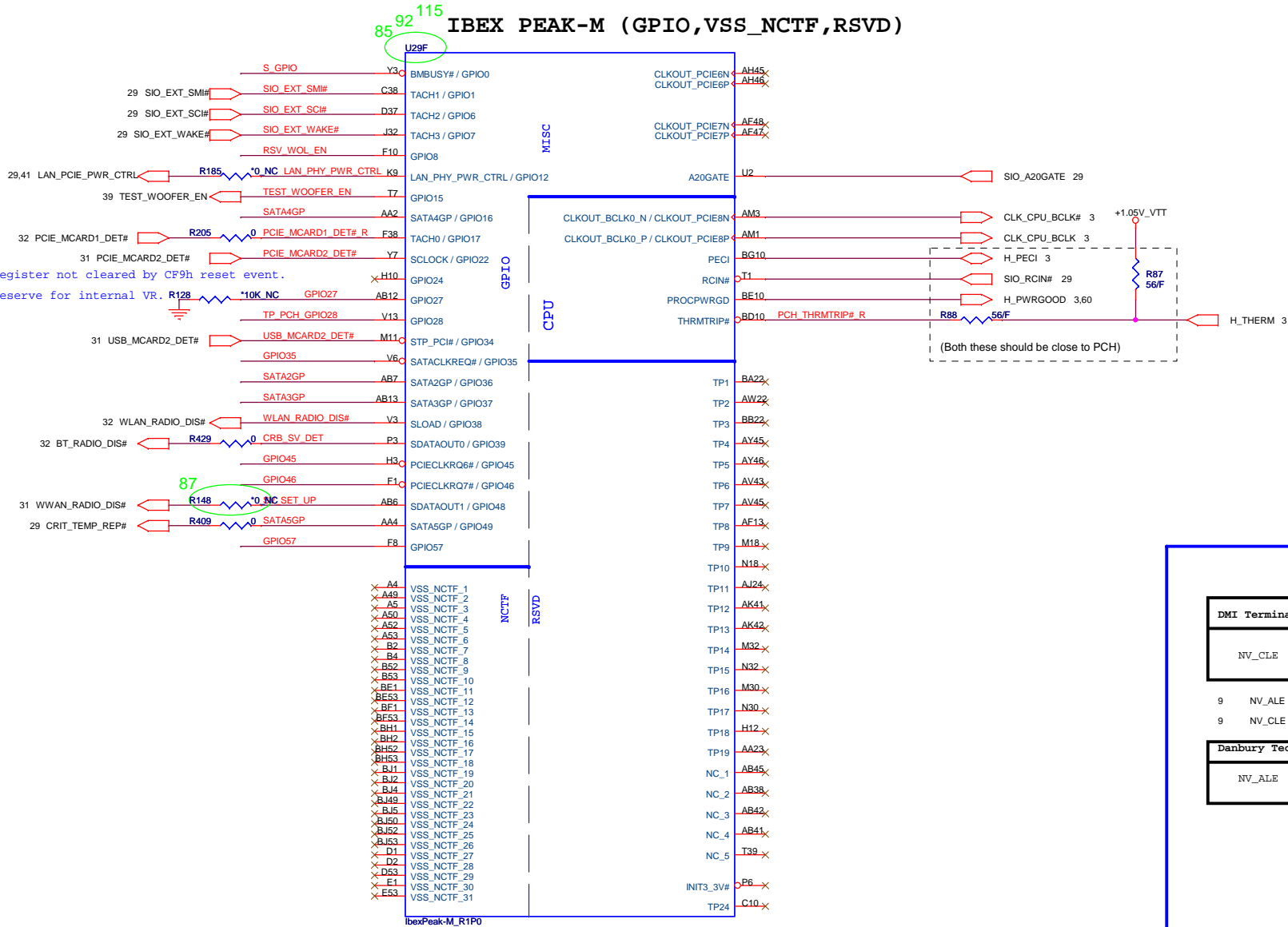
## IBEX PEAK-M (PCI,USB,NVRAM)

## IBEX PEAK-M (PCI-E,SMBUS,CLK)

Place TX DC blocking caps close PCH.



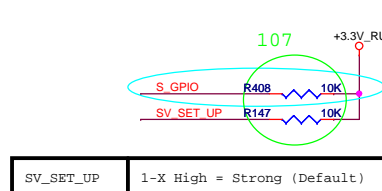
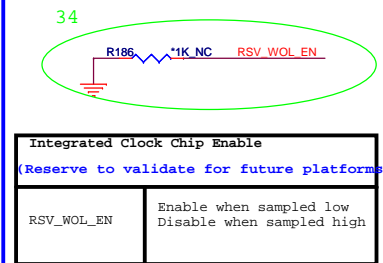
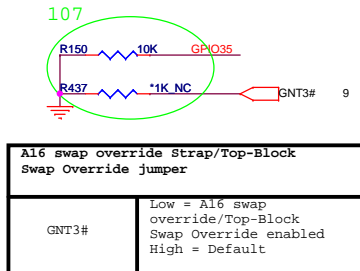
# IBEX PEAK-M (GPIO,VSS\_NCTF,RSVD)



DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH



Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

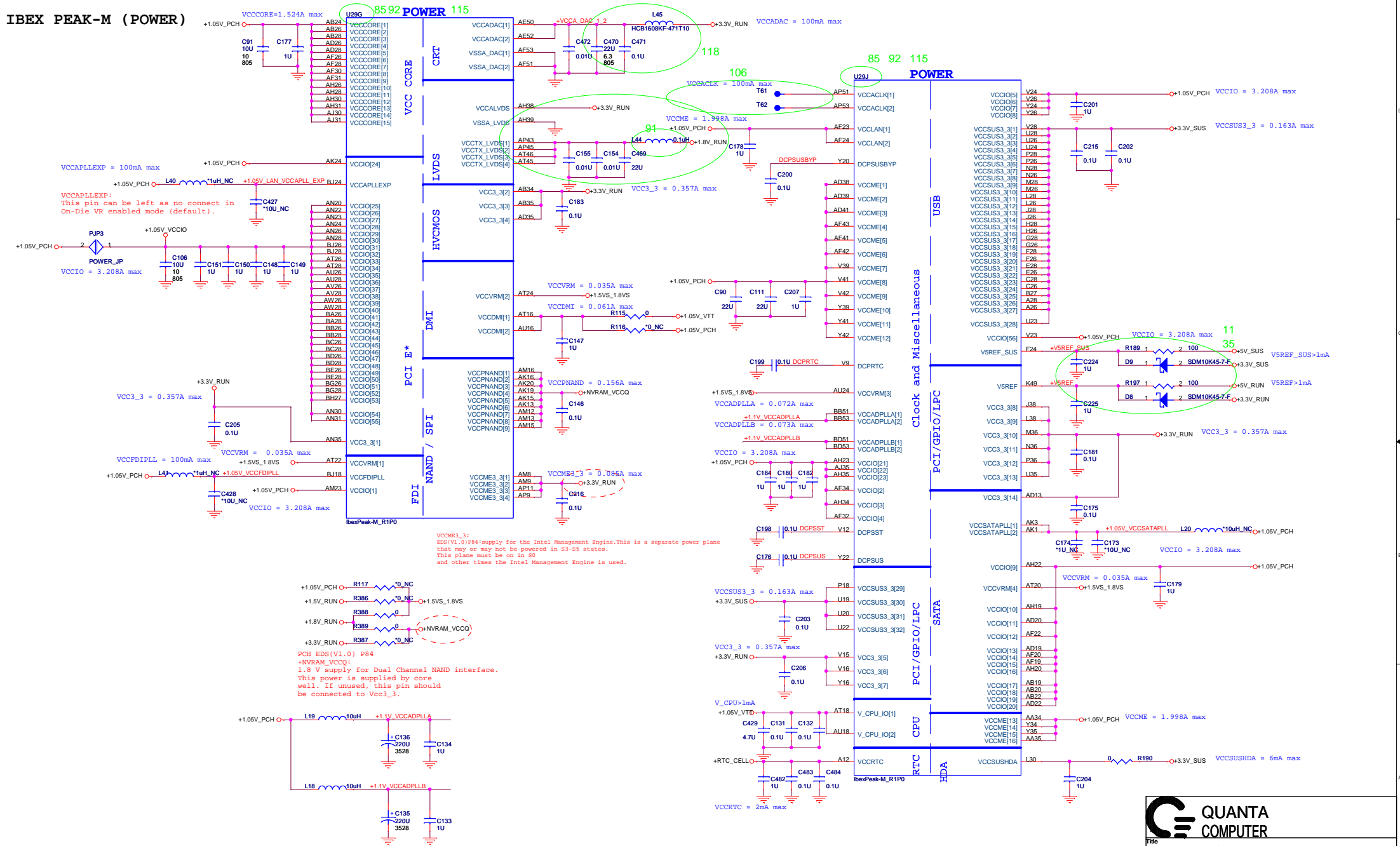


**6**

**BMBUSY#:**  
If not used, require a weak pull-up (8.2- 10 kΩ) to Vcc3.3.  
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

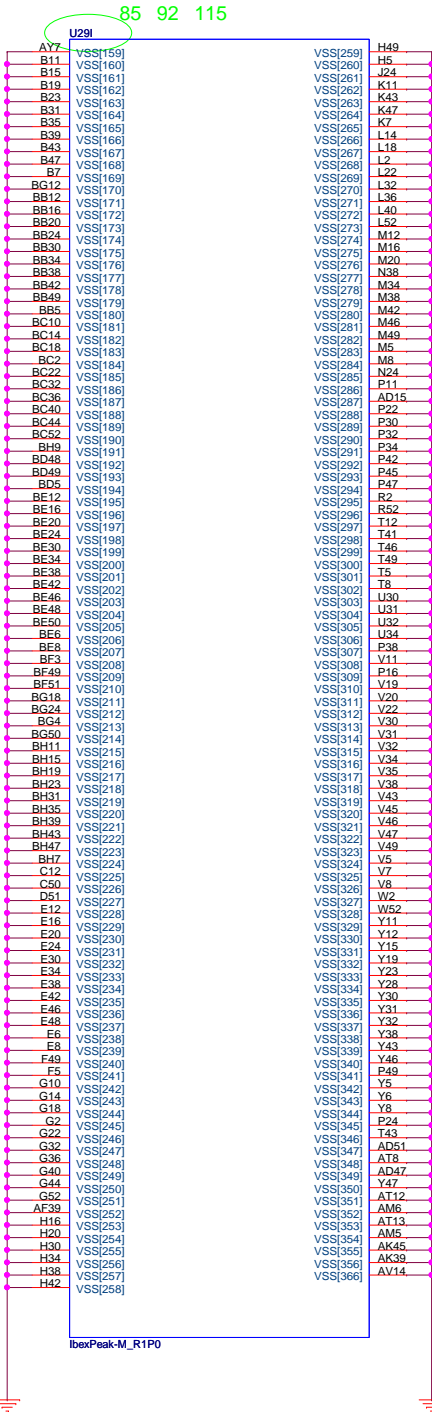
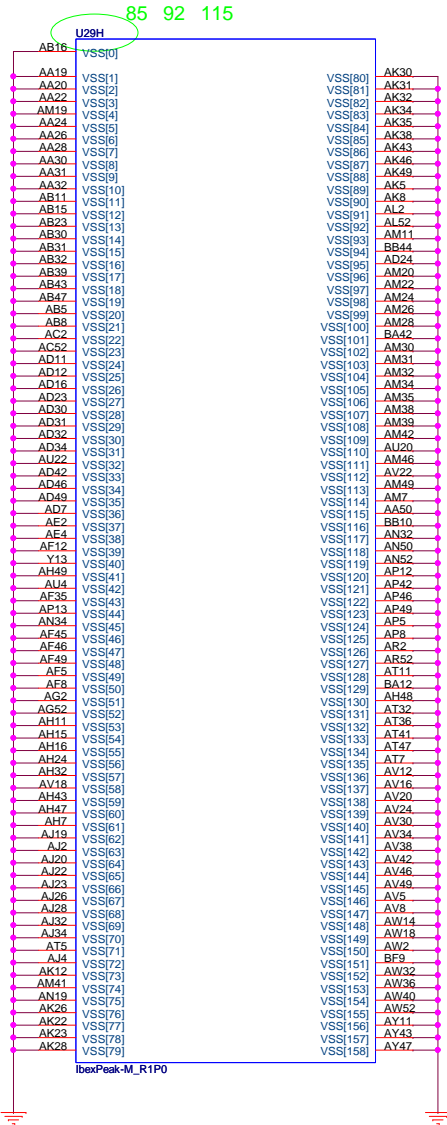
**BMBUSY#:(Intel feedback)**  
Follow CRB checklist, 1K is for intel BIOS validation purpose.

## IBEX PEAK-M (POWER)

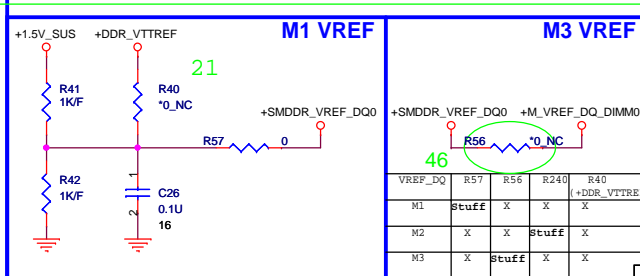
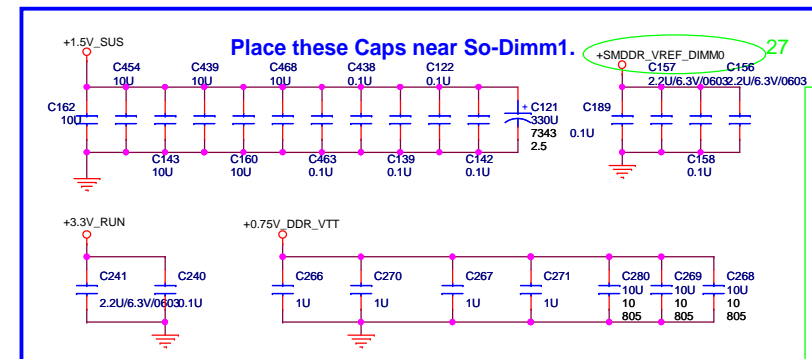


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IBEX PEAK-M 5/6			
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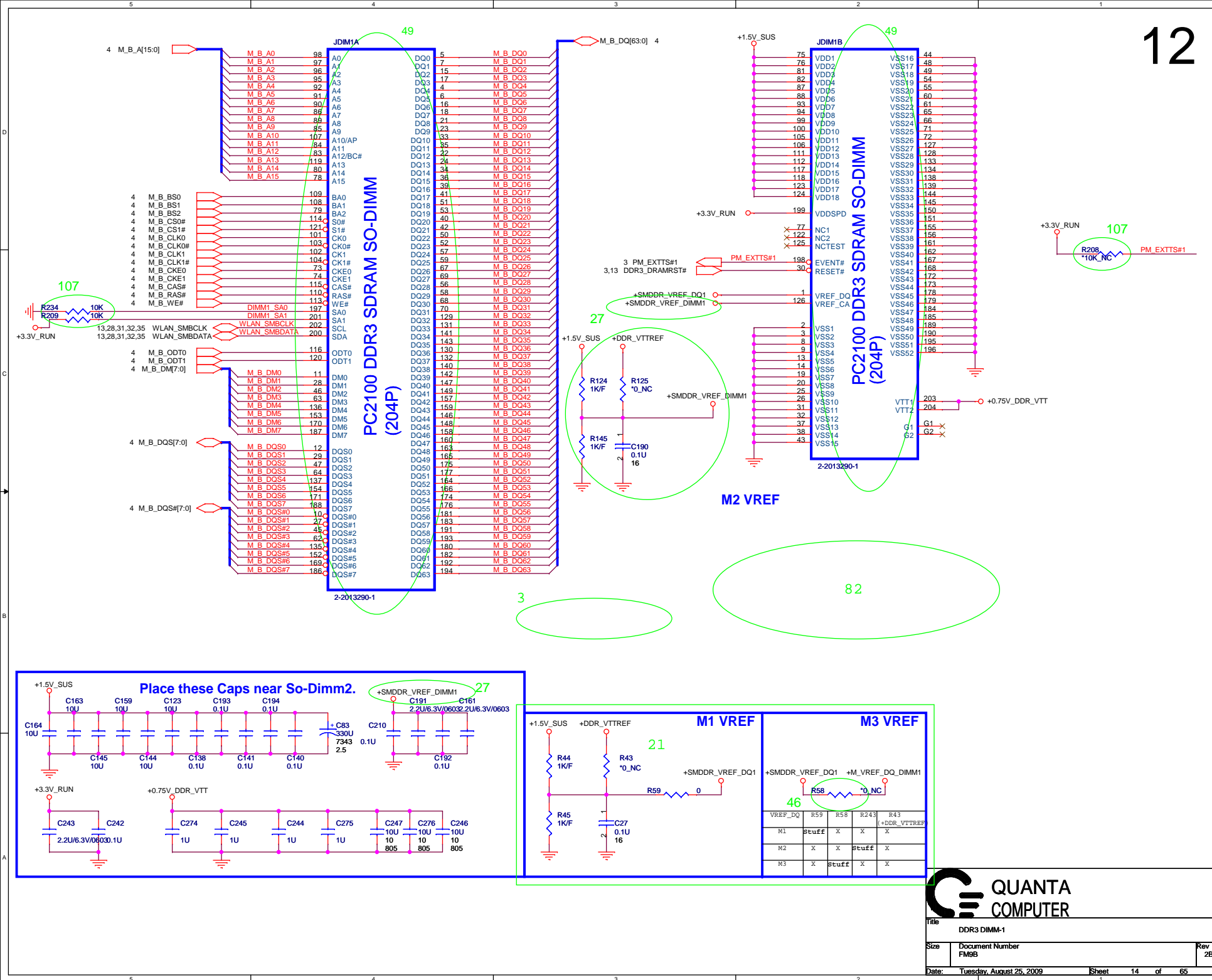
IBEX PEAK-M (GND)



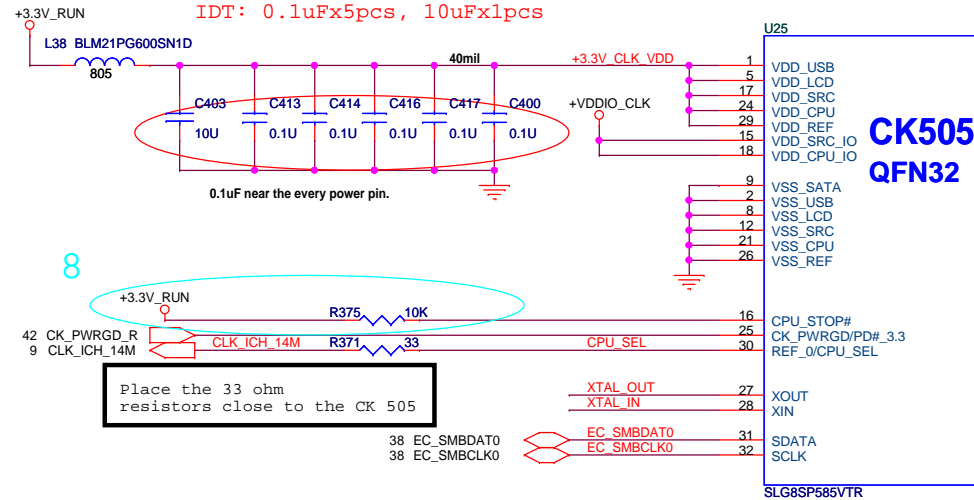
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Size		Document Number			Rev		28
		FM9B					
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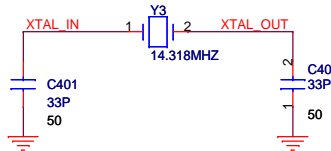
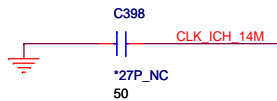




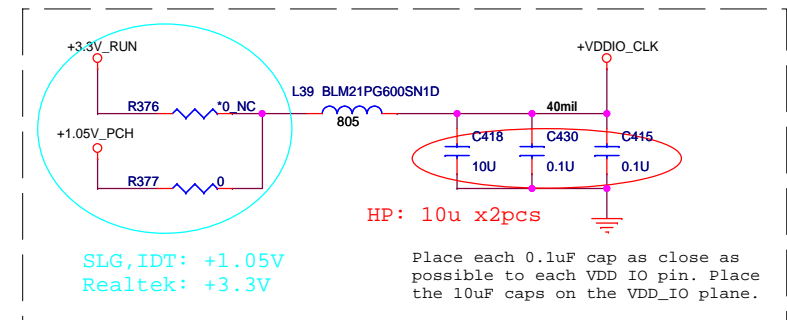
Realtek: 0.1uF x 6pcs, 22uF x 1pcs  
 IDT: 0.1uF x 5pcs, 10uF x 1pcs



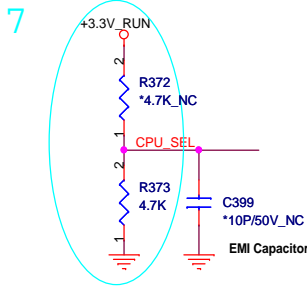
Add capacitor pads for improving WWAN.



Realtek: 0.1uF x 3pcs, 22uF x 1pcs  
 IDT: 0.1uF x 2pcs, 10uF x 1pcs



+VDDIO\_CLK:  
 SLG date sheet (V0.2) P15: Min 1.05V, Max 3.465V.  
 Realtek date sheet (V1.2) P11: Min 1.05V, Max 3.3V.  
 IDT date sheet (V0.7) P10: Min 0.9975V, Max 3.465V.




PIN	30	CPU_0	CPU_1
0 (default)		133MHz	133MHz
1 (0.7V-1.5V)		100MHz	100MHz

CPU\_SEL:  
 SLG date sheet (V0.2) P15:  
 High Voltage: Min 0.7V, Max 1.5V.  
 Low Voltage: Min Vss-0.3V, Max 0.35V.  
 Realtek date sheet (V1.2) P11:  
 High Voltage: Min 0.7V, Max 1.5V.  
 Low Voltage: Min Vss-0.3V, Max 0.35V.  
 IDT date sheet (V0.7) P10:  
 High Voltage: Min 0.7V, Max 1.5V.  
 Low Voltage: Min Vss-0.3V, Max 0.35V.




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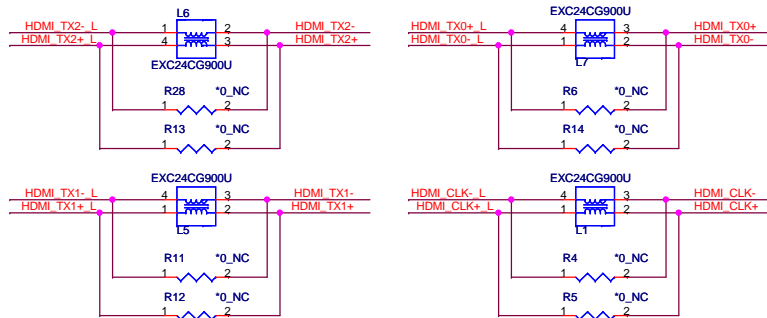
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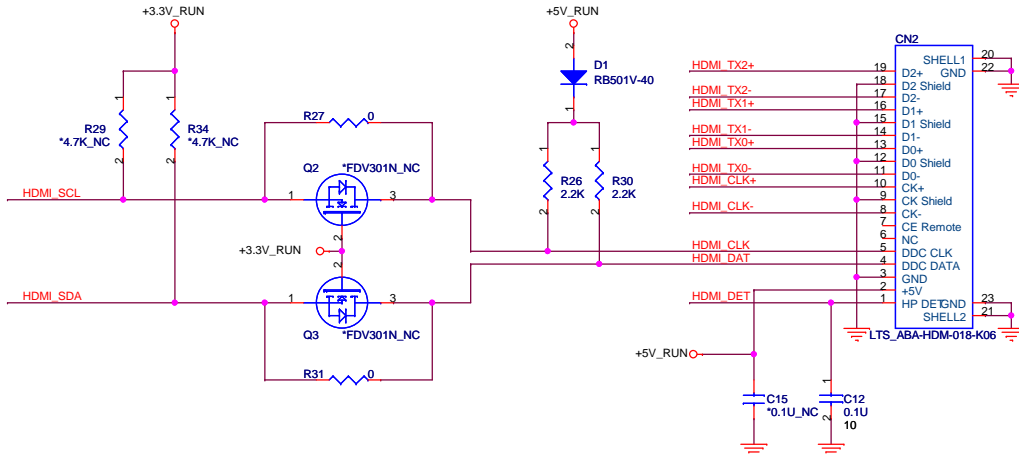
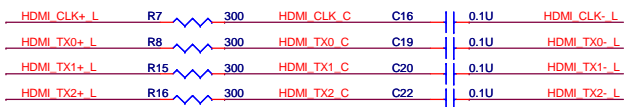
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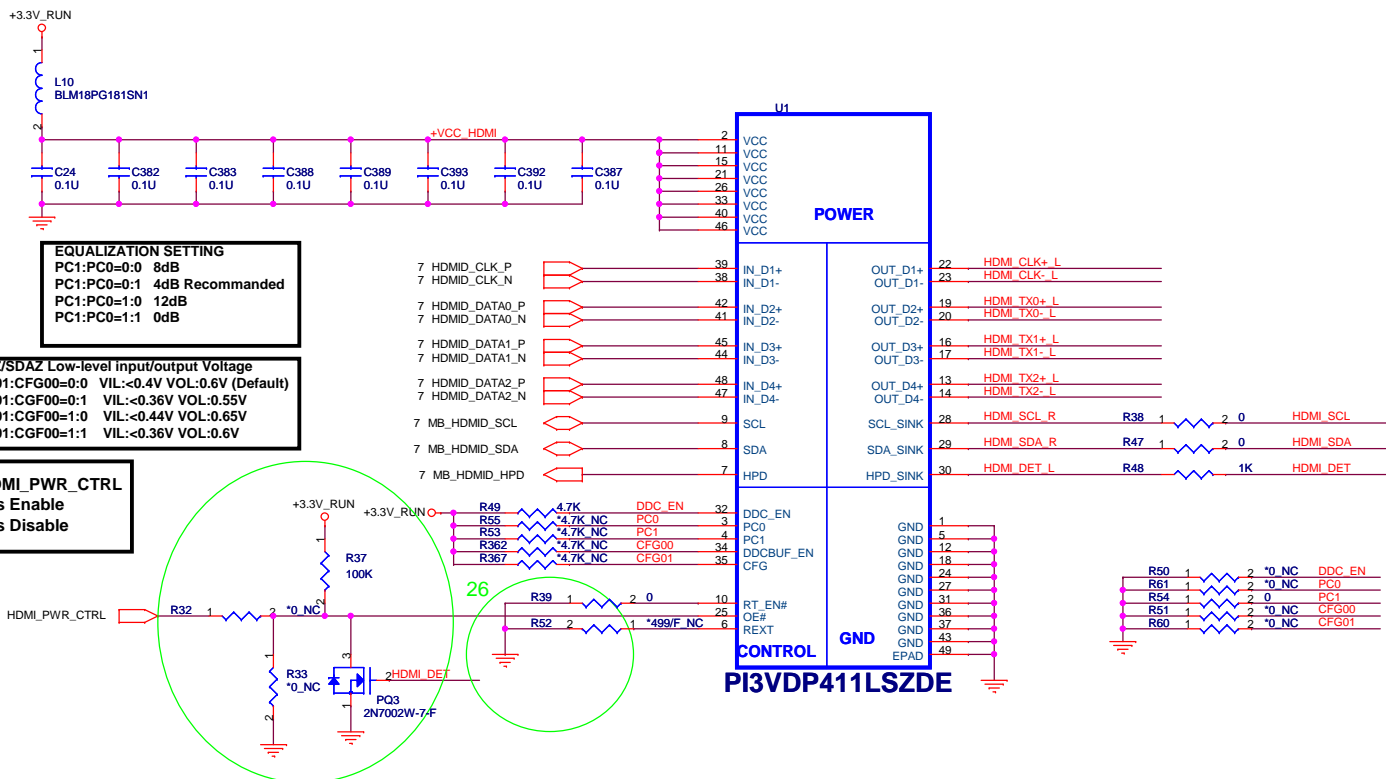




Reserve for EMI and close to HDMI CONN

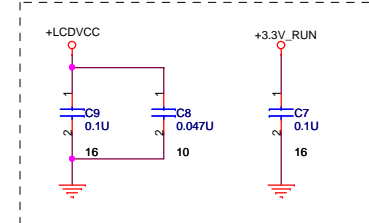
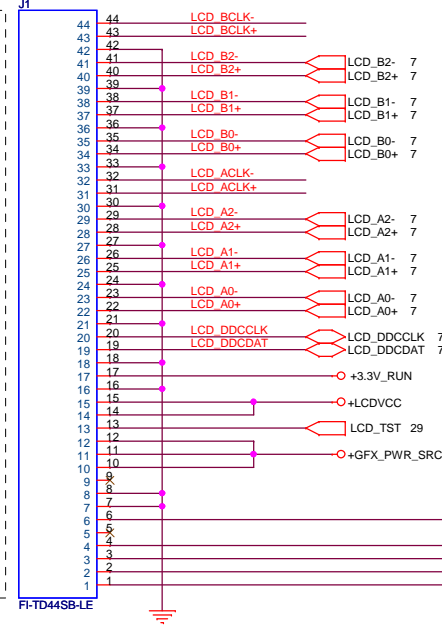
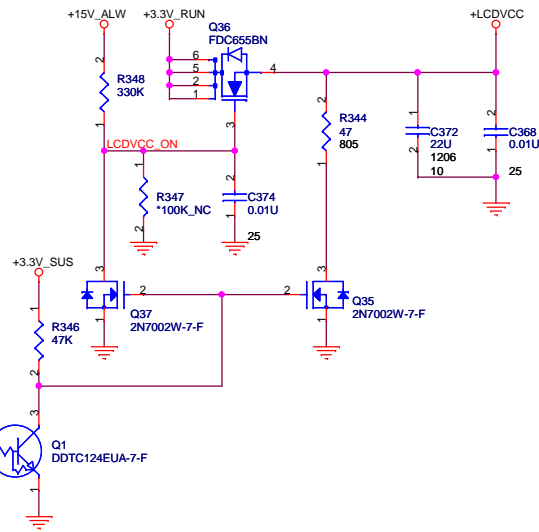
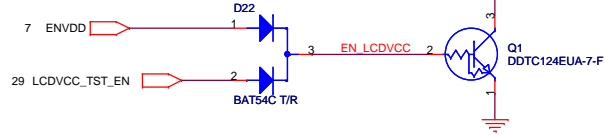


HDMI

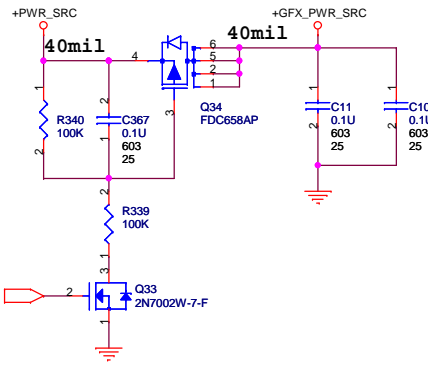
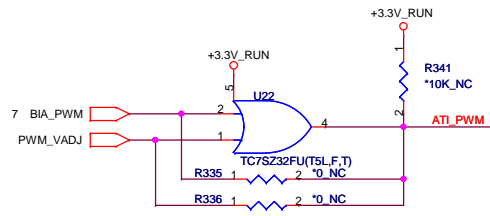


QUANTA  
COMPUTER

Support the new imbedded diagnostics.

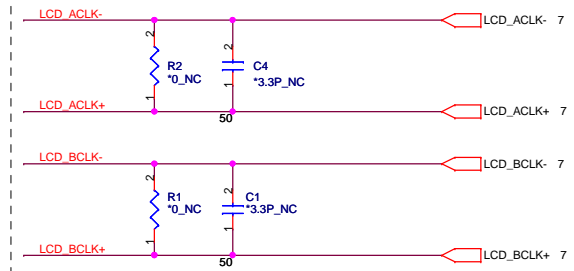


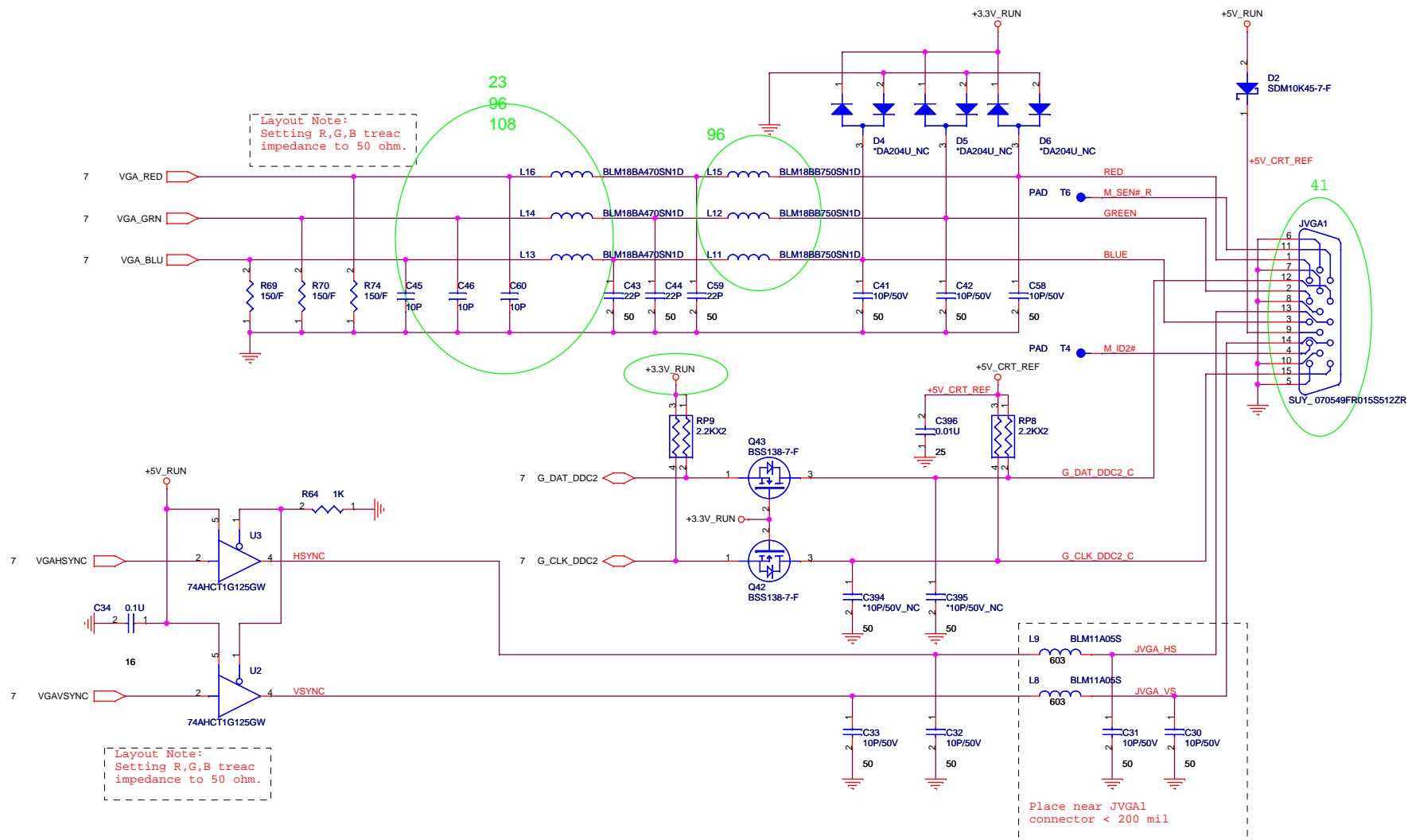
Address : A9H --Contrast  
AAH --Backlight



Shunt capacitors on LVDS for improving WWAN.

LCD B0-	C13	1	2	*3.3P NC	50	LCD B0+
LCD B1-	C3	1	2	*3.3P NC	50	LCD B1+
LCD B2-	C2	1	2	*3.3P NC	50	LCD B2+
LCD A0-	C6	1	2	*3.3P NC	50	LCD A0+
LCD A1-	C5	1	2	*3.3P NC	50	LCD A1+
LCD A2-	C14	1	2	*3.3P NC	50	LCD A2+

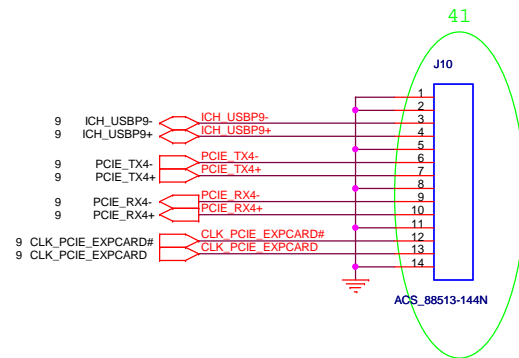
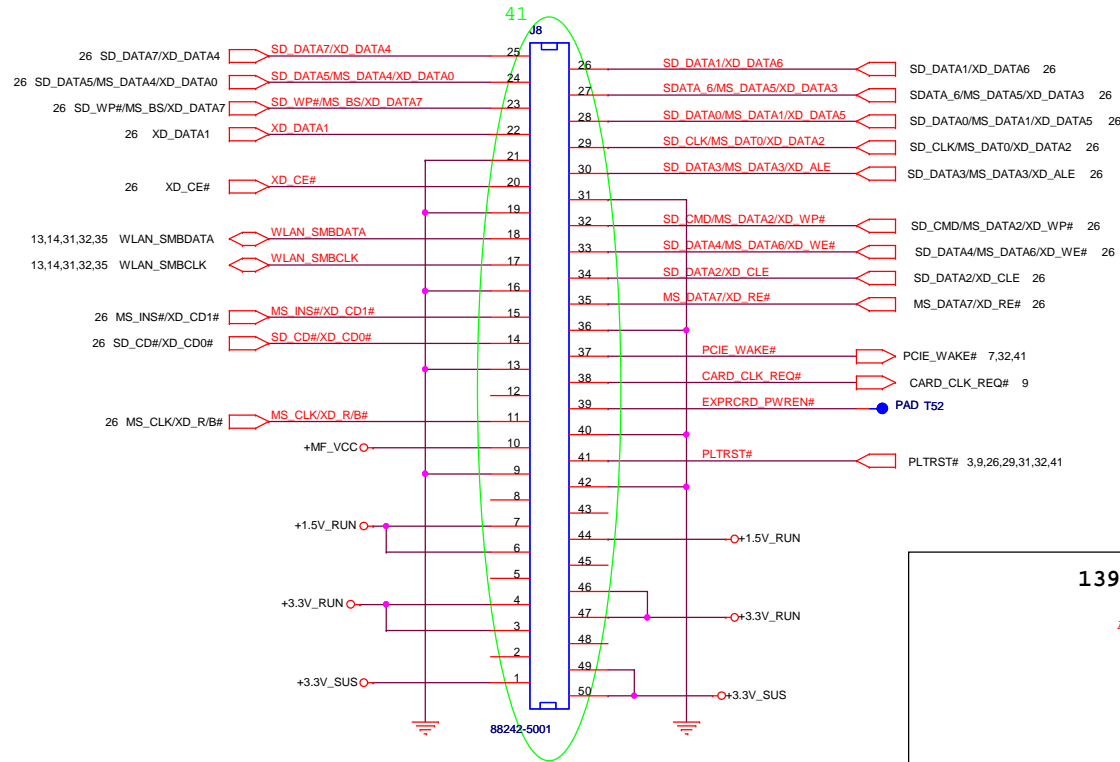






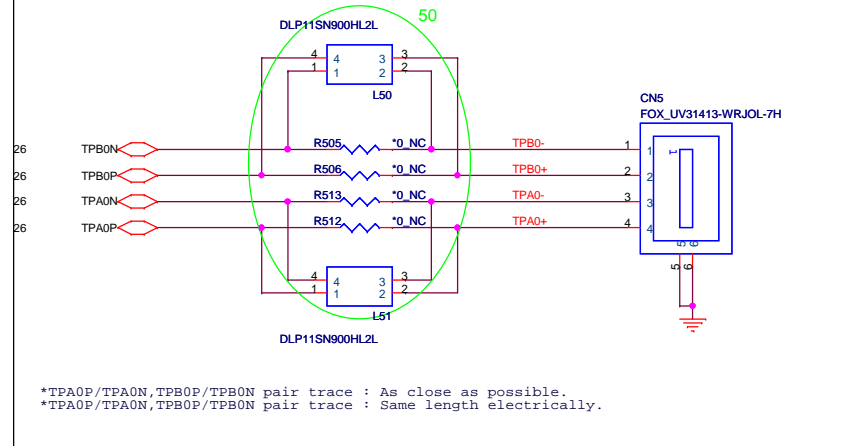
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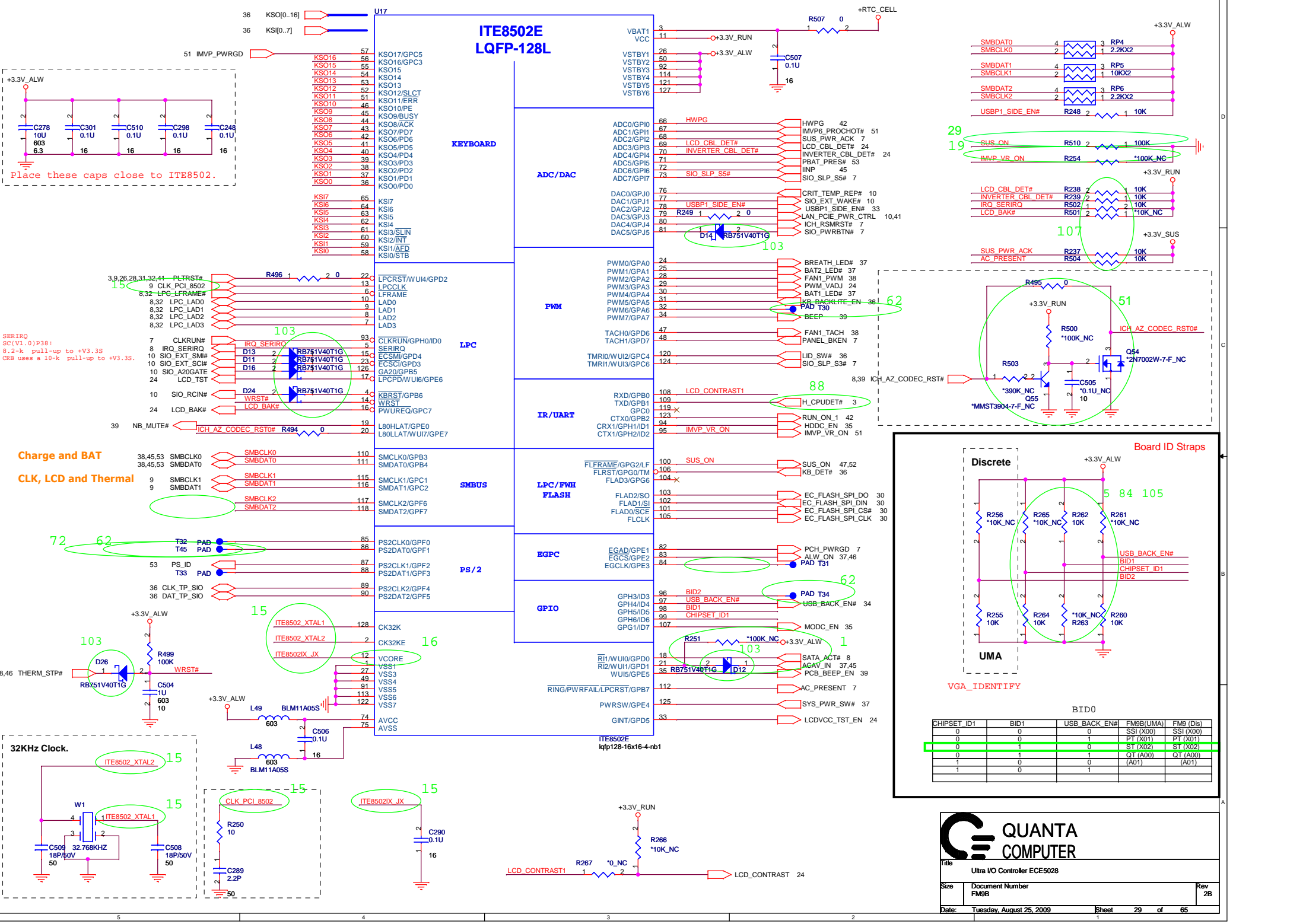
# Express Card/CARD READER




## 1394 CONNECTOR

AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.





BID0					
CHIPSET_ID1	BID1	USB_BACK_EN#	FM9B(UMA)	FM9(Ds)	
0	0	0	SSI (X00)	SSI (X00)	
0	0	1	PT (X01)	PT (X01)	
0	1	0	ST (X02)	ST (X02)	
1	1	1	QT (A00)	QT (A00)	
1	0	0	(A01)	(A01)	



**QUANTA**  
COMPUTER

Title

Ultra I/O Controller ECE5028

Size

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FM9B

Date:

Tuesday, August 25, 2009

Sheet

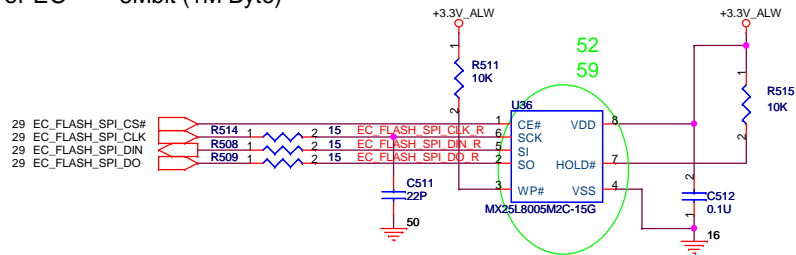
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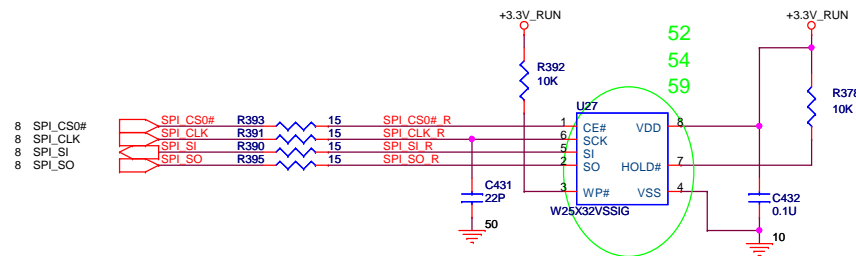
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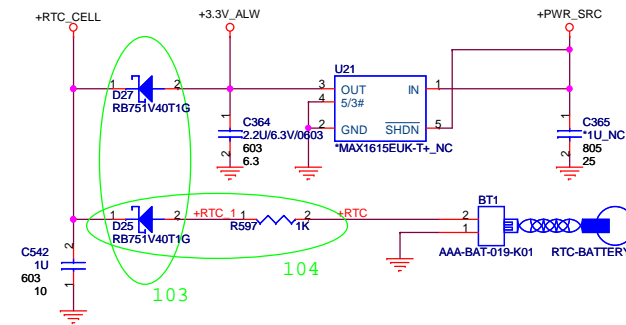
# For EC 8Mbit (1M Byte)



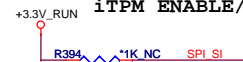
# For PCH 32Mbit (4M Byte)



# RTC BATTERY



# iTPM ENABLE/DISABLE



TPM Function	R712
Enable	Mount
Disable	NC (Default)

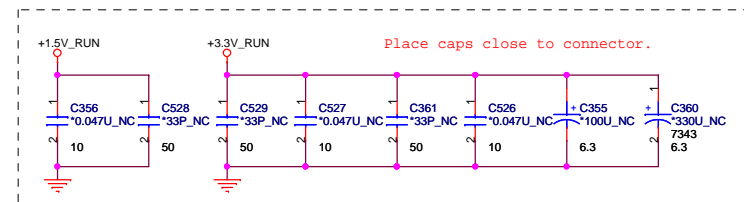
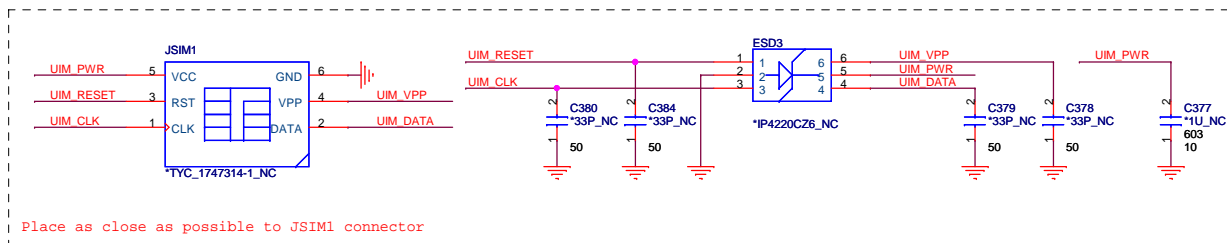
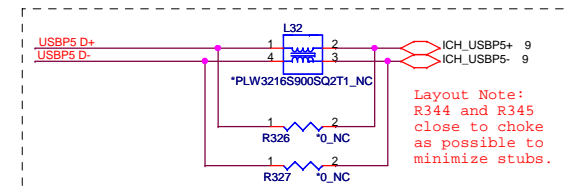
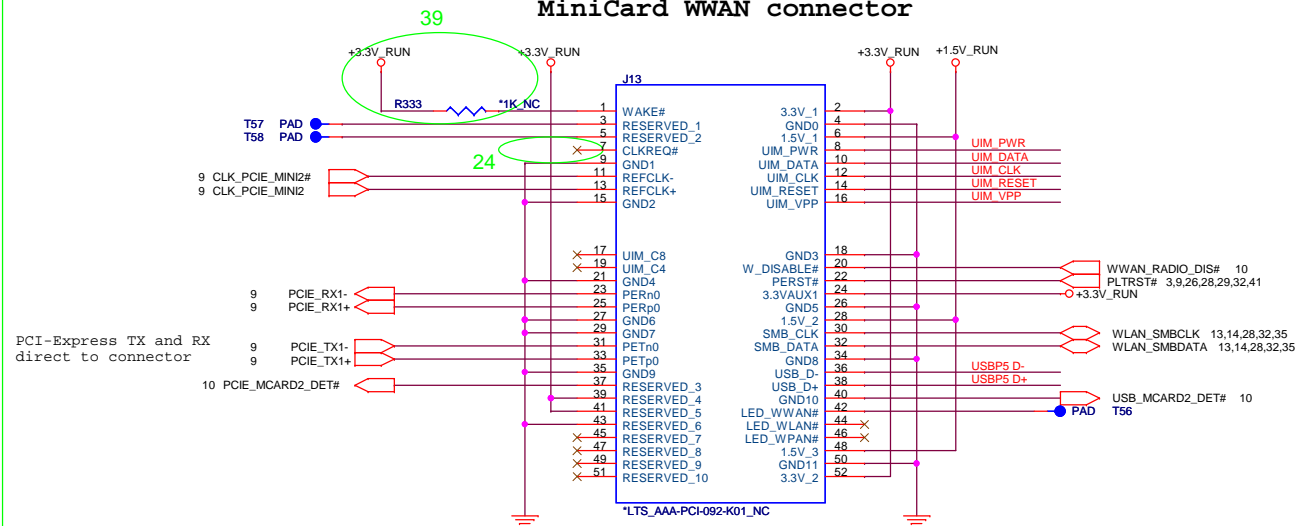


Ultra I/O Controller ECE5028

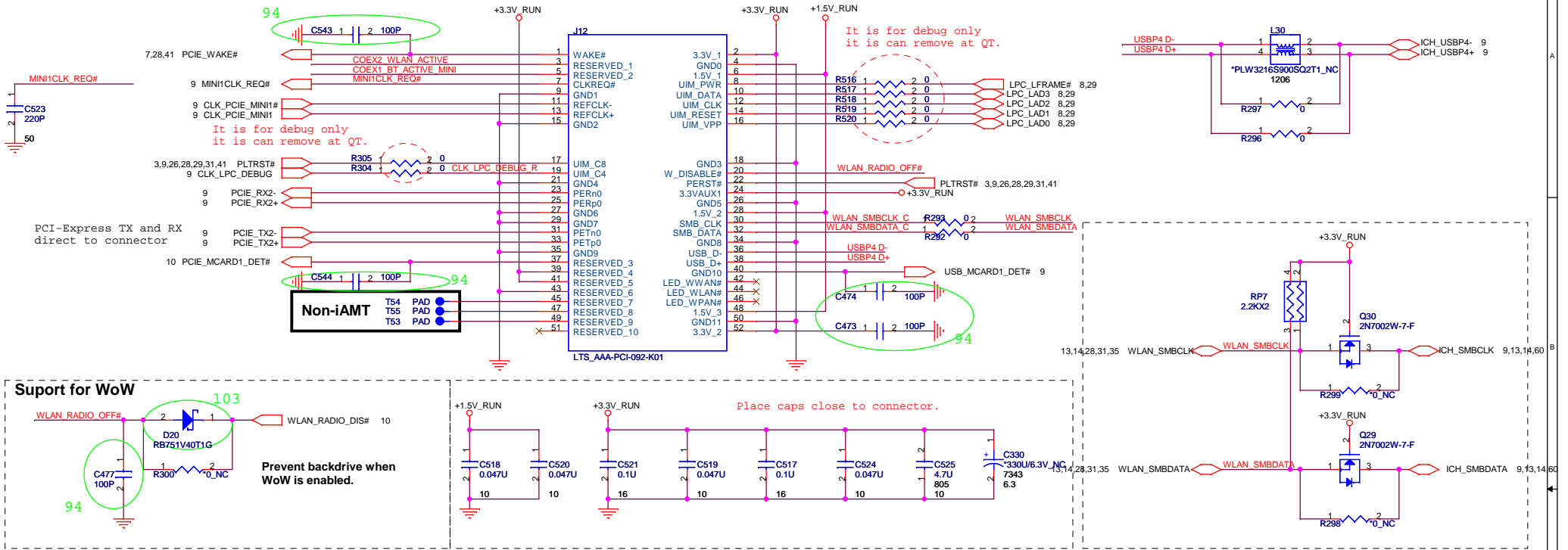
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FM9B

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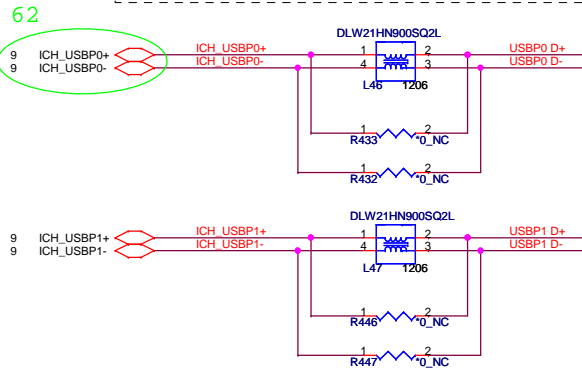
## MiniCard WWAN connector



# MiniCard WLAN connector

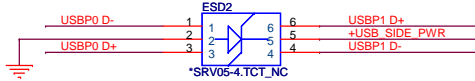


External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently



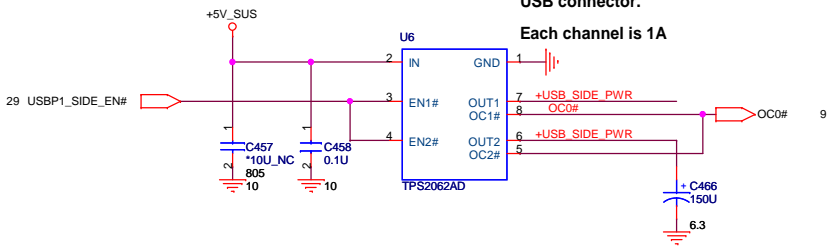
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

Place ESD diodes as close as USB connector.



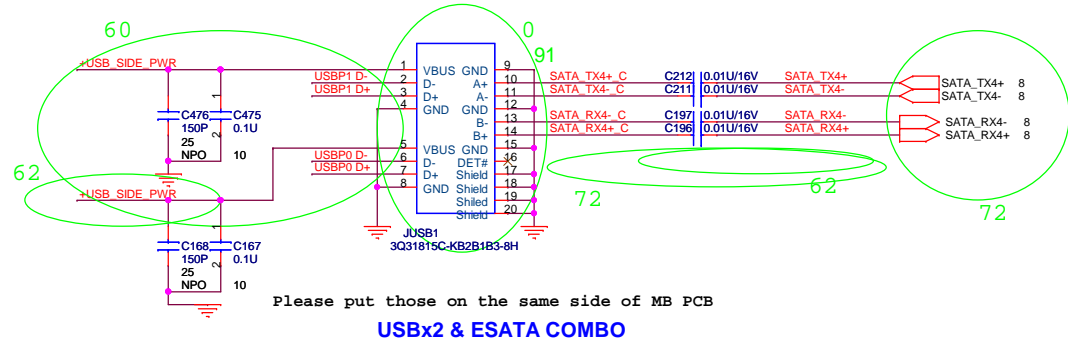
Place one 150uF cap by each USB connector.

Each channel is 1A



## Side External USBX2

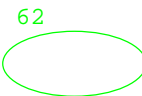
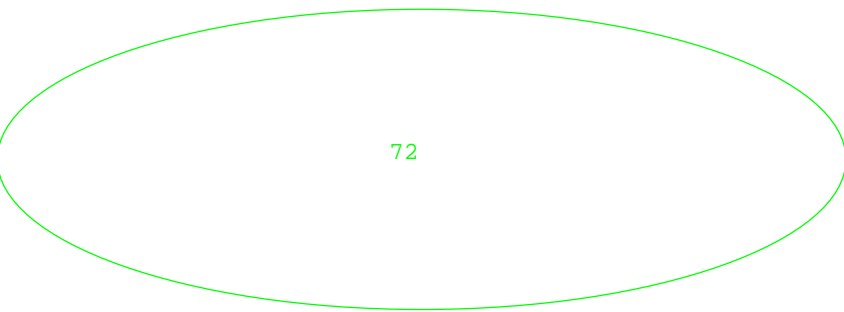
PN is old, Because New Part can't ready before SST build.



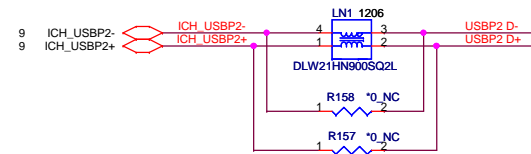
## USB BUS SW



## E-SATA Re-driver

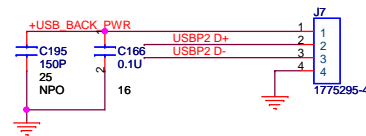
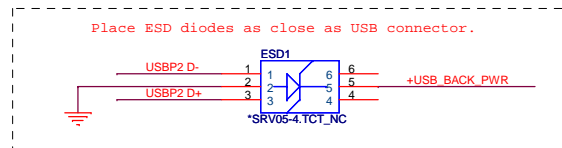
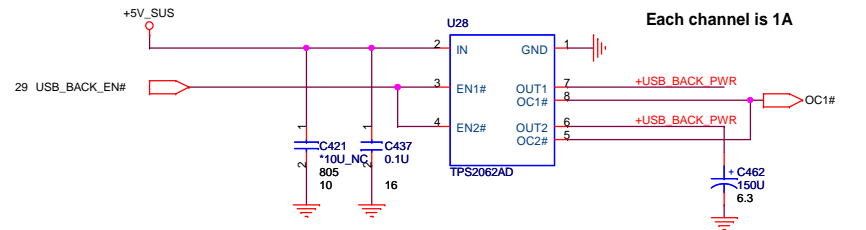


Title			SERIAL PORT & USB
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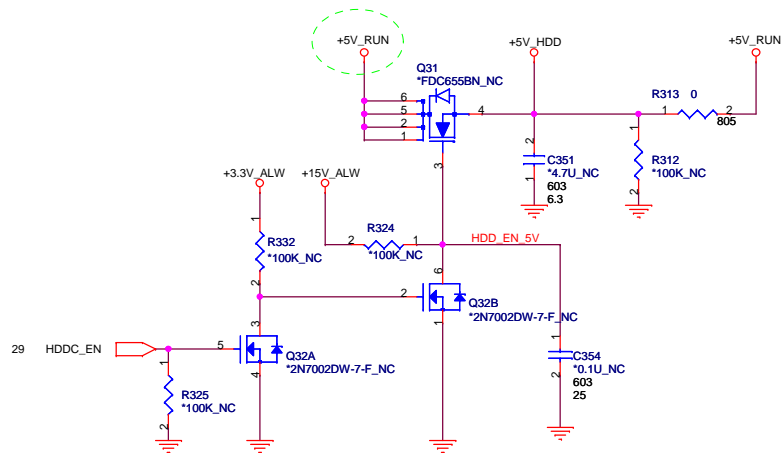
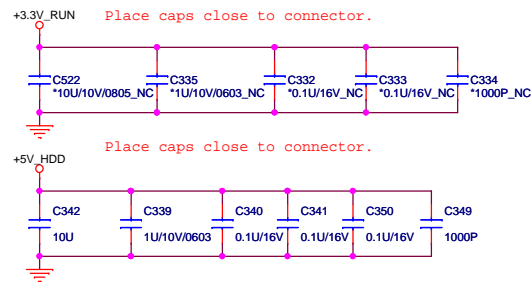
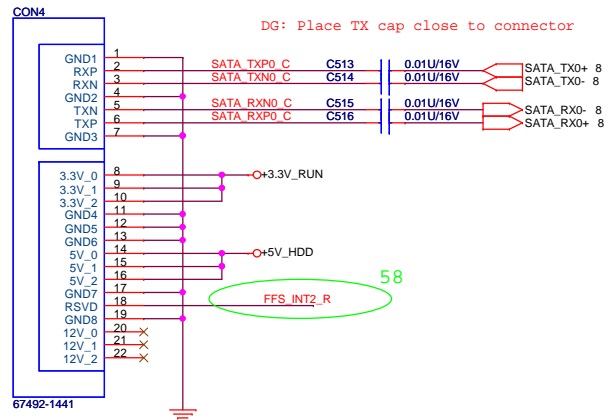
Place one 150uF cap by each  
USB connector.

Each channel is 1A

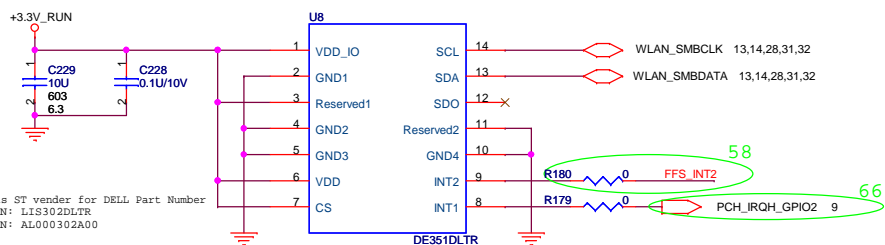


Title		
Right USB		
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## SATA Connector.

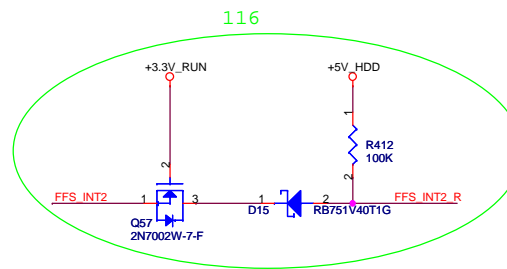
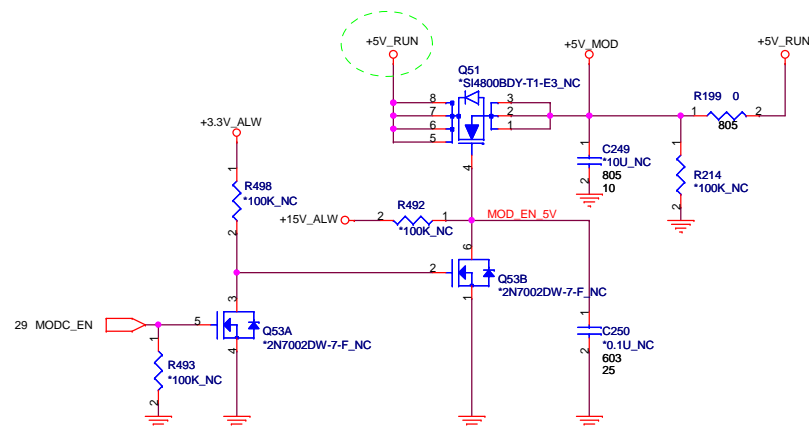
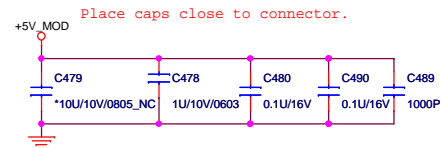
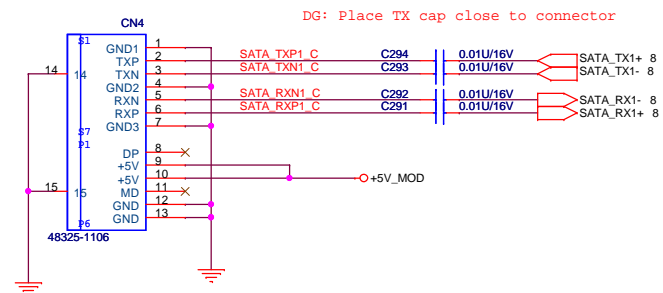


## 3-axis Fall Sensor (HDD data protector)



DE351DL is ST vendor for DELL Part Number  
Vendor PN: L1S302DLTR  
Quanta PN: AL000302A00

## ODD Connector



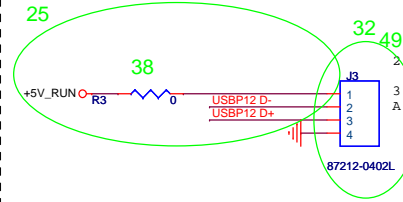
Title			SATA (HDD&CD_ROM)
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	FM9B	2B	
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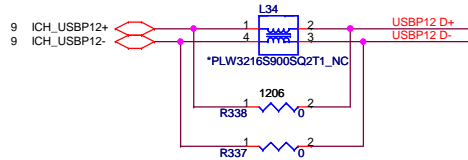


## Touch Screen Module

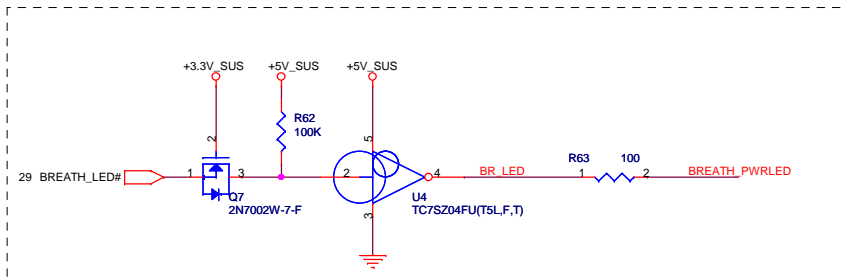
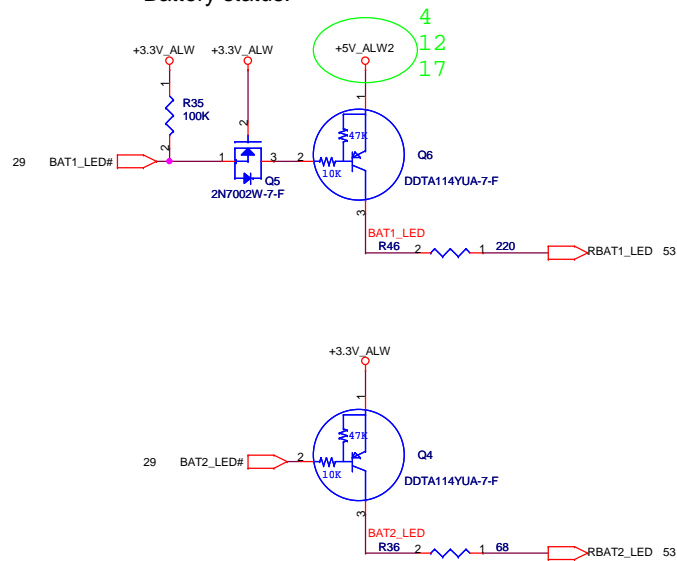
- Note:
1. VBUS IND:VBUS indication should be supplied to single the DuoSense to connect According to the USB 2.0 specification. A GND voltage from the host should indicate a connection.
  2. Maximum cable resistance on VCC, GND should be 150m ohm.
  3. FPC cable should support 12MHz USB singles. A tri-state should indicate no connection.



Need check the connector footprint and symbol.



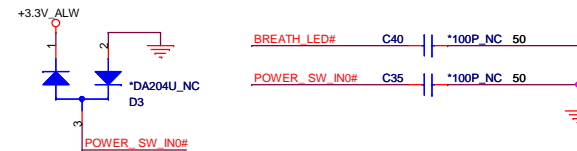
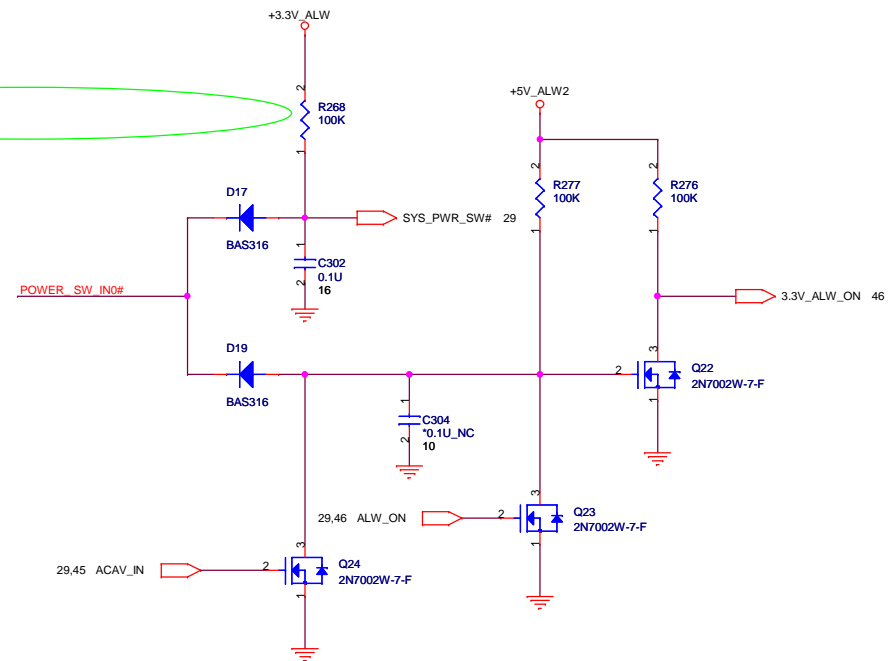
### Battery status.

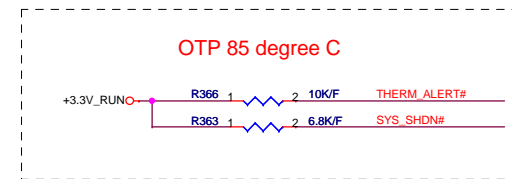
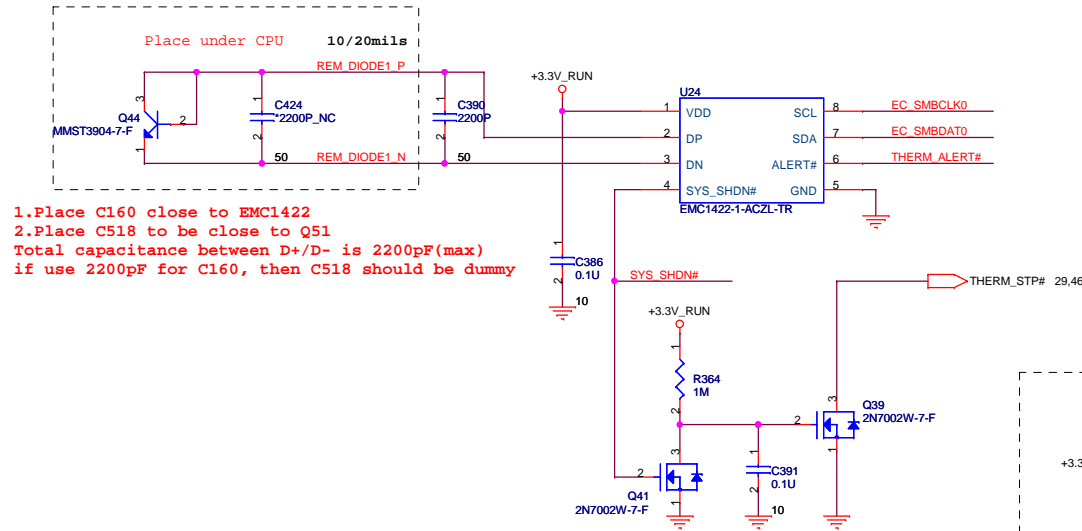
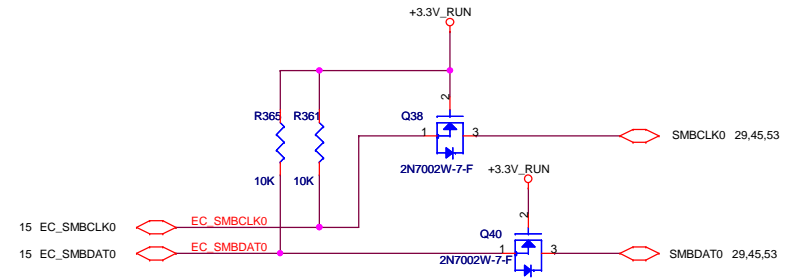
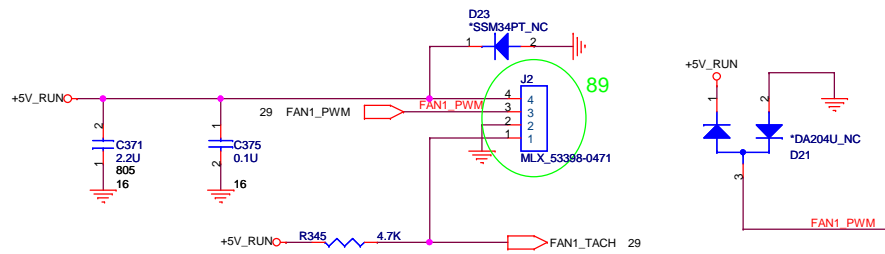


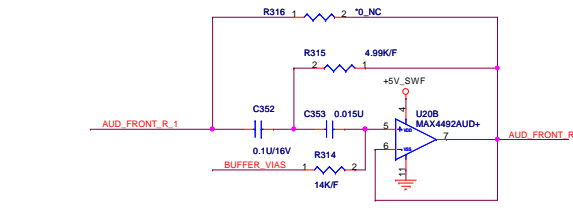
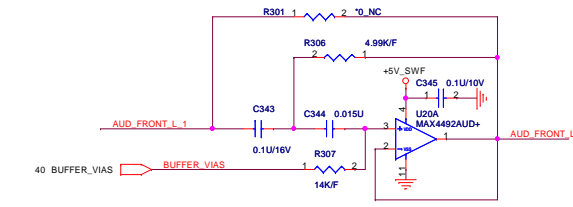
### Power button Cable



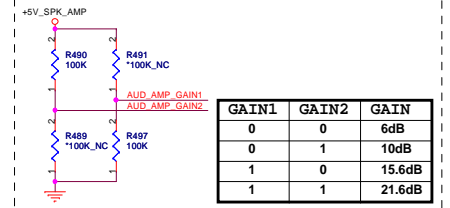
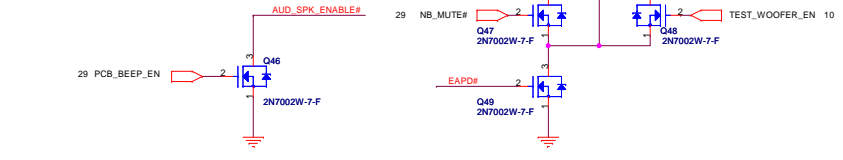
### 3VALW ON POWER LOGIC



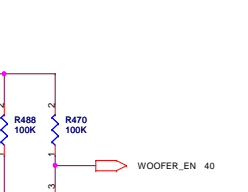
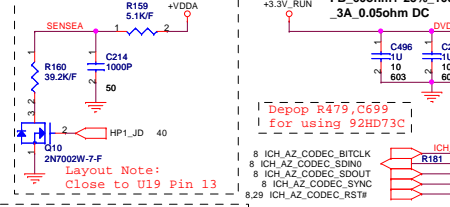
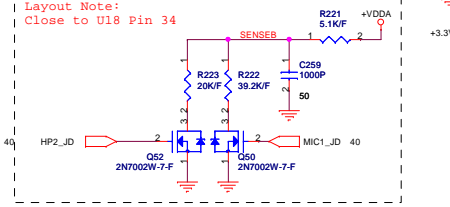
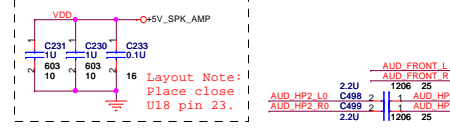




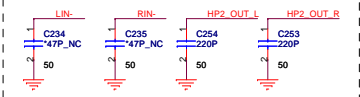
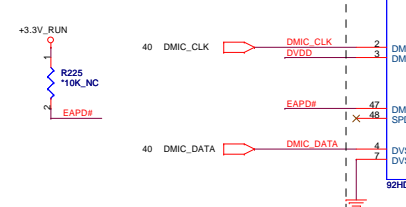
EAPD#	NB_MUTE#	TEST_WOOFER_EN	AUD_SPK_ENABLE#	SUB_MUTE#
0	0	0	H	L
0	0	1	H	L
0	1	0	H	L
0	1	1	H	L
1	0	0	H	L
1	0	1	H (Disable SPK)	H (Test Woofer)
1	1	0	L (Test SPK)	L (Disable Woofer)
1	1	1	L	H



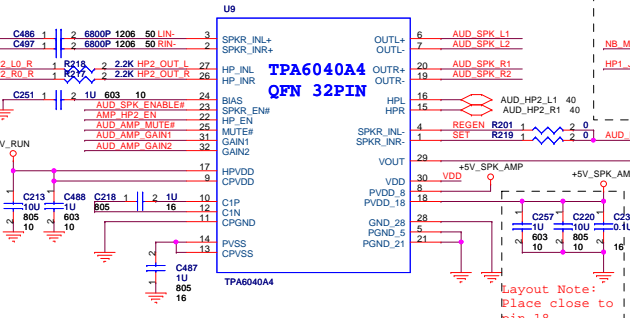
GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



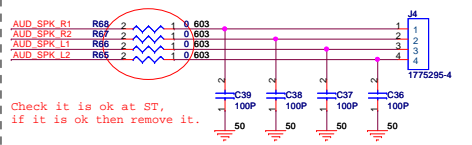
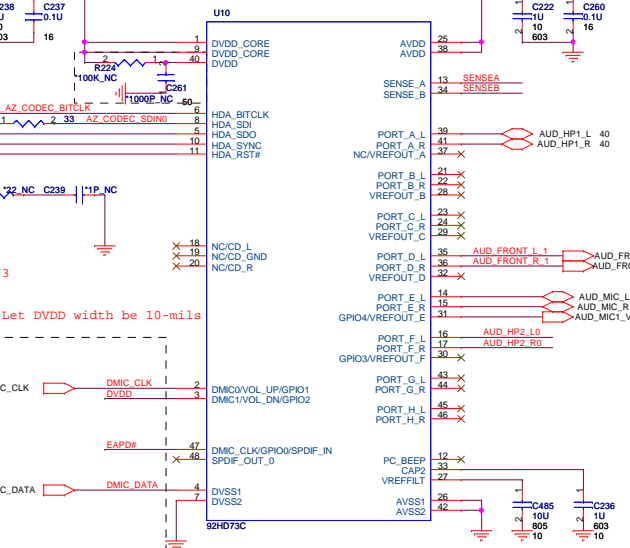
Depop R477,R478,R484,R473  
Pop R476,R480,R483,R475  
for using 92HD73C  
R476,R483 close to U19, Let DVDD width be 10-mils



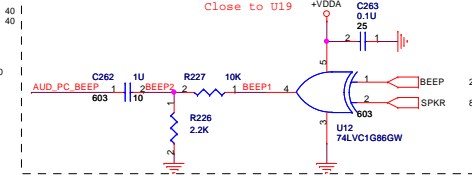
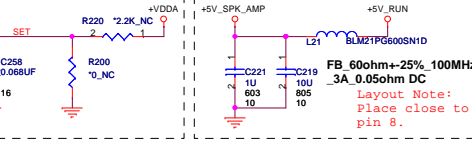
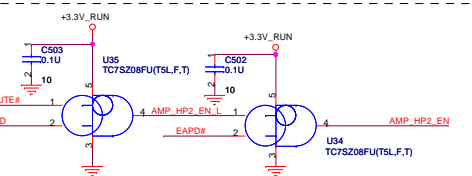
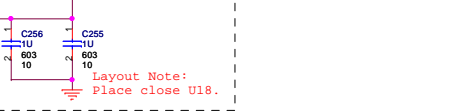
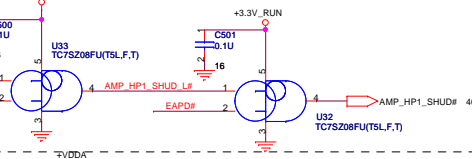
### INTERNAL SPEAKER AMP



### AZALIA (HD) CODEC

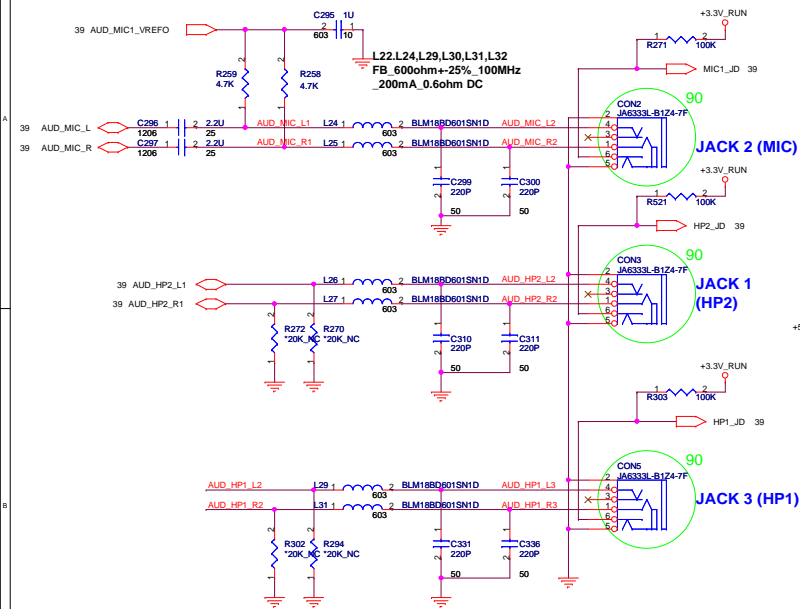


Check it is ok at ST.  
if it is ok then remove it.

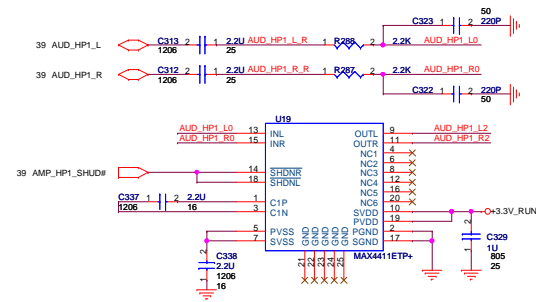
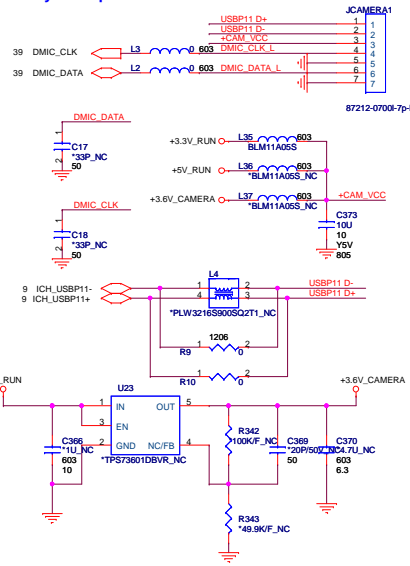


File	Azalia CODEC	Rev	2B
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**Headphone Jack**  
**Stereo MIC Jack**

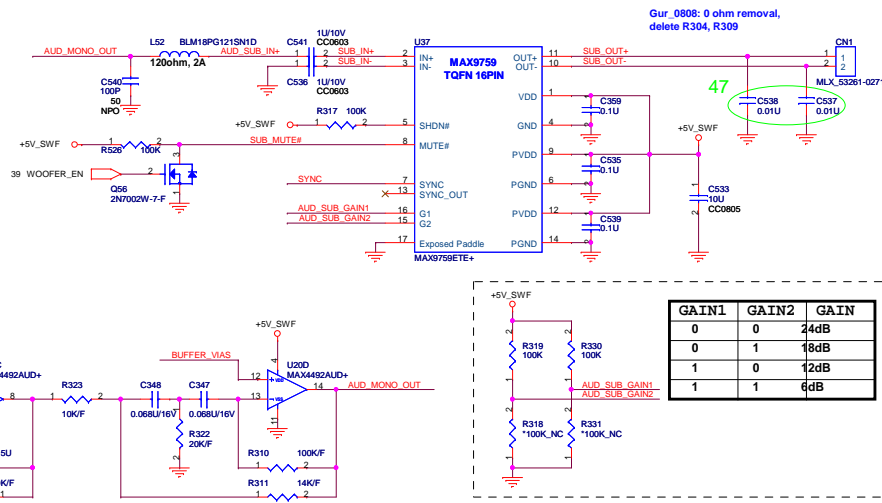


## Array Microphone & Camera

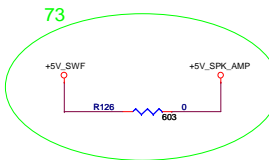


## INTERNAL SUBWOOFER AMP

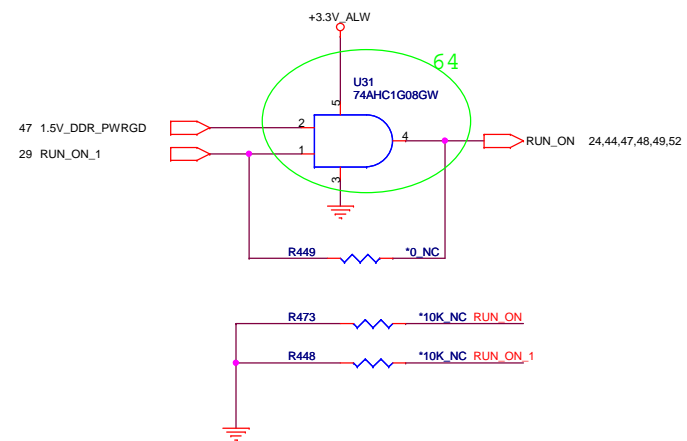
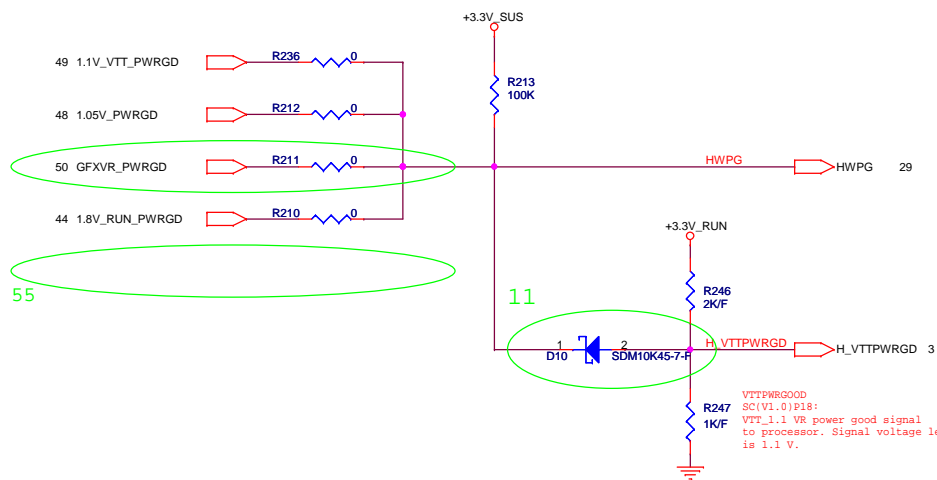
SYNC	Condition
VDD	Spread-spectrum mode with fS = 1200kHz $\pm$ 70kHz.
GND	Fixed-frequency mode with fS = 1100kHz.
FLOAT	Fixed-frequency mode with fS = 1500kHz.
Clocked	Fixed-frequency mode with fS = external clock frequency.




GAIN1	GAIN2	GAIN
0	0	24dB
0	1	18dB
1	0	12dB
1	1	6dB

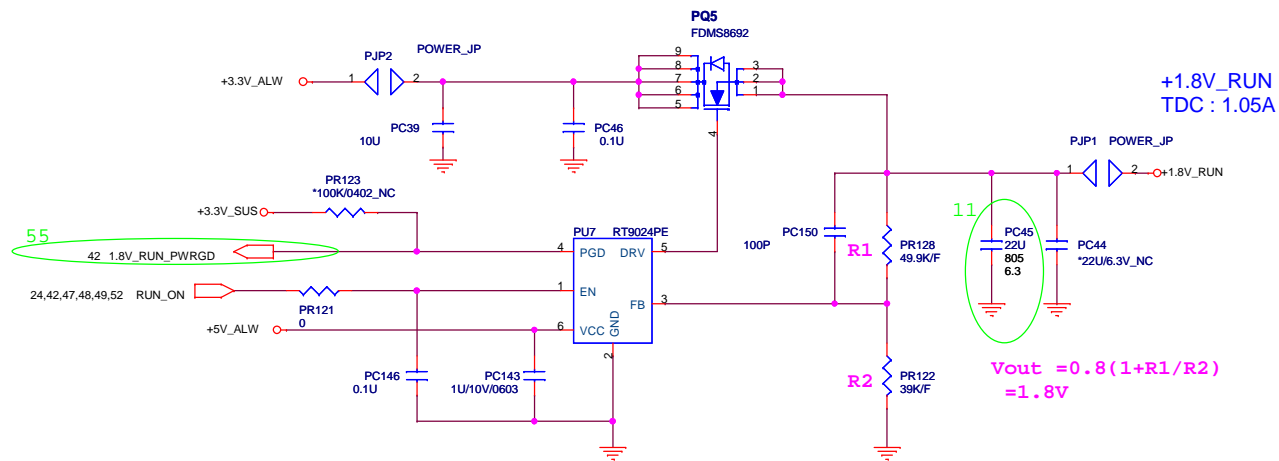






	1	2	3	4	5
A					
B					
C					
D					
	1	2	3	4	5

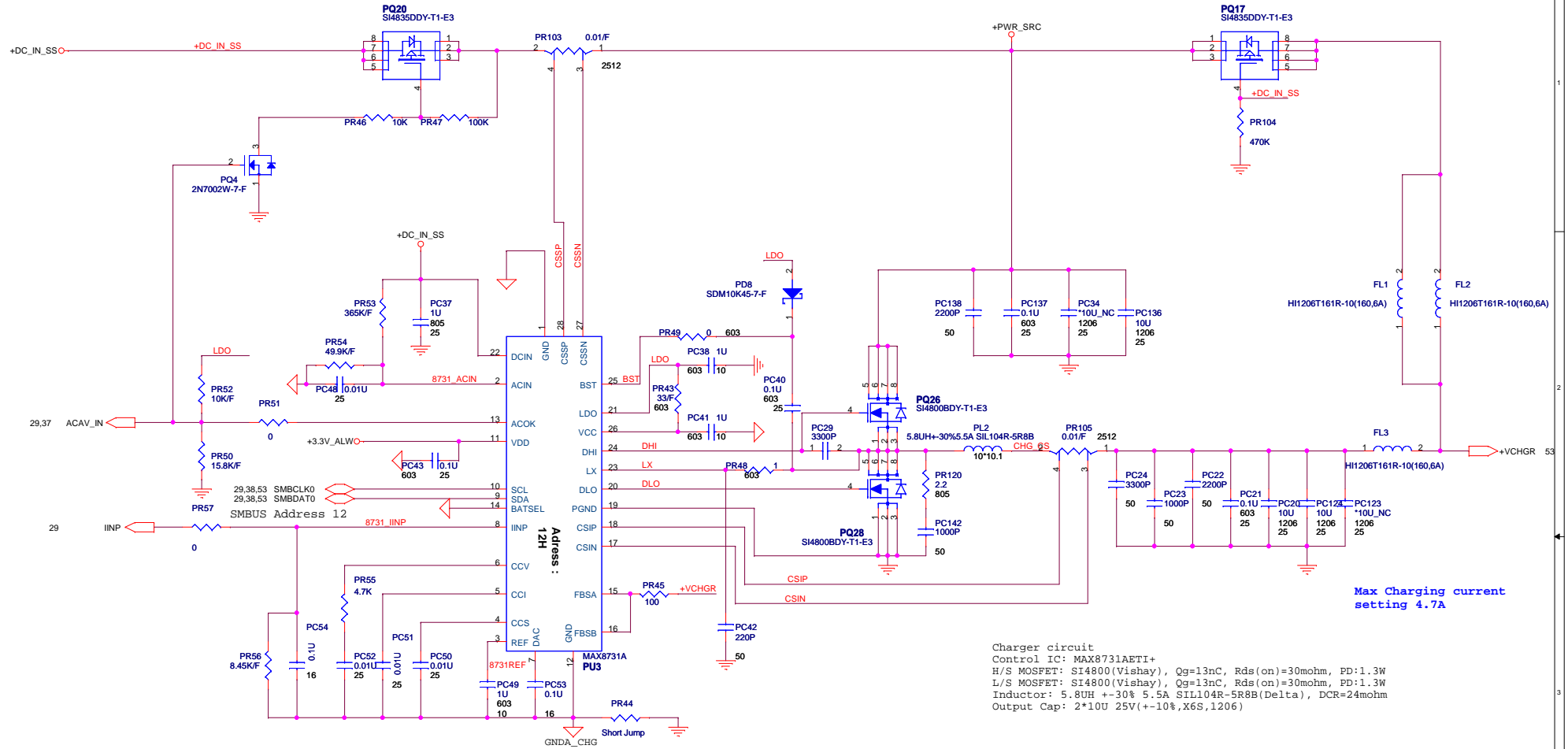
 <div>QUANTA COMPUTER</div>		
Title Battery Selector		
Size	Document Number FM9B	Rev 2B
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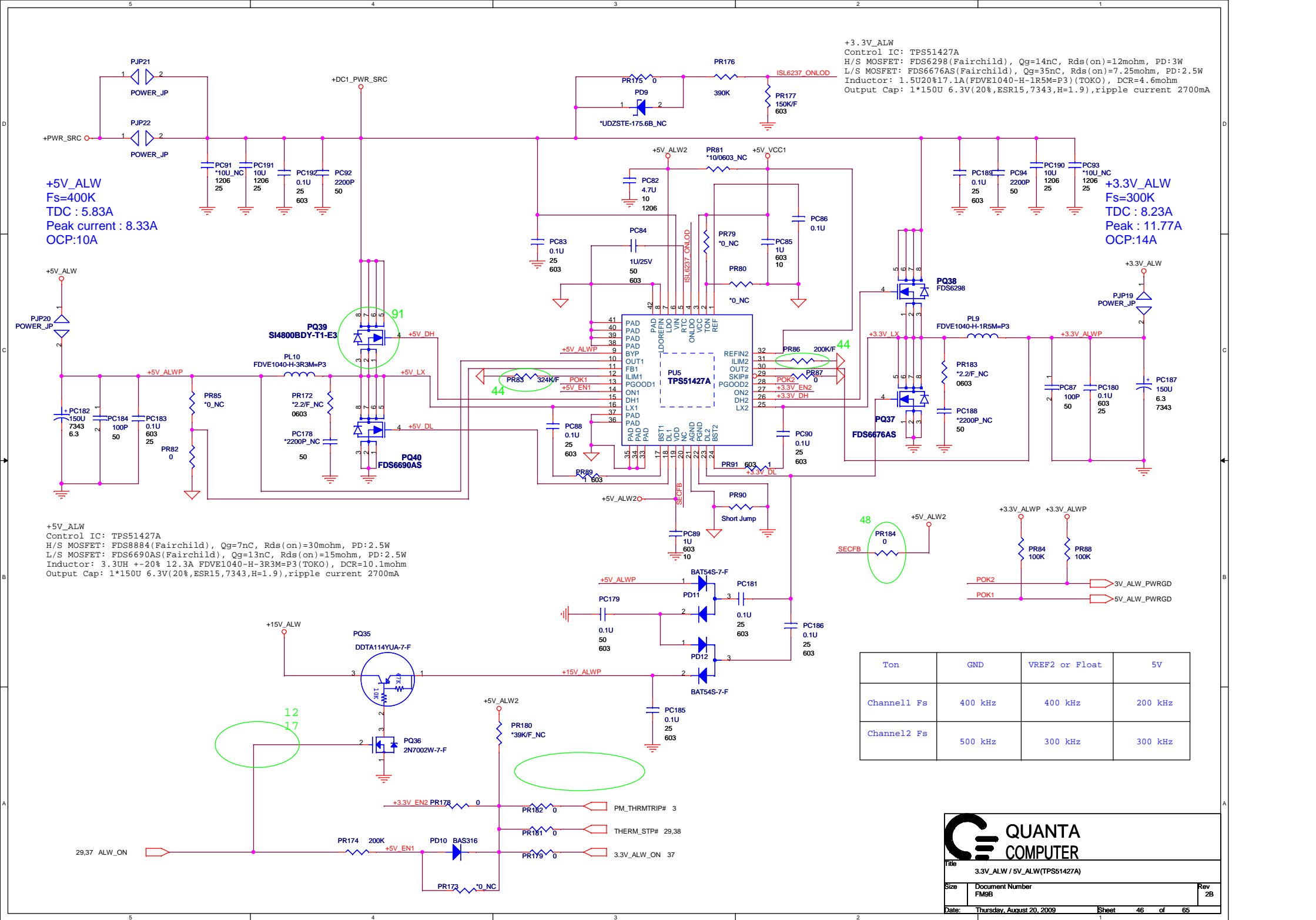


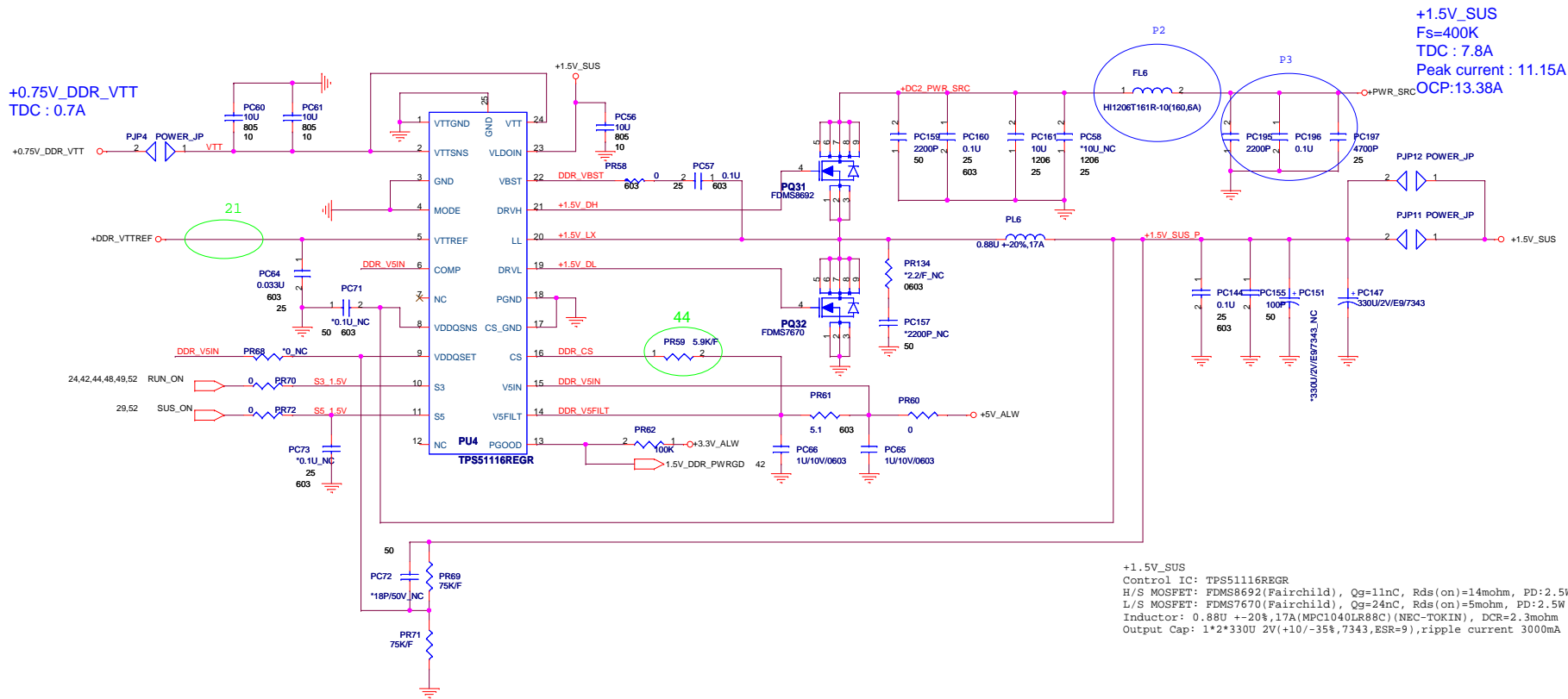
Continuous current : 13A  
Rds(on) : 18mohm

Continuous current : 13A  
Rds(on) : 18mohm



Title			Charger (MAX8731)
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VDDQ and VTT discharge control

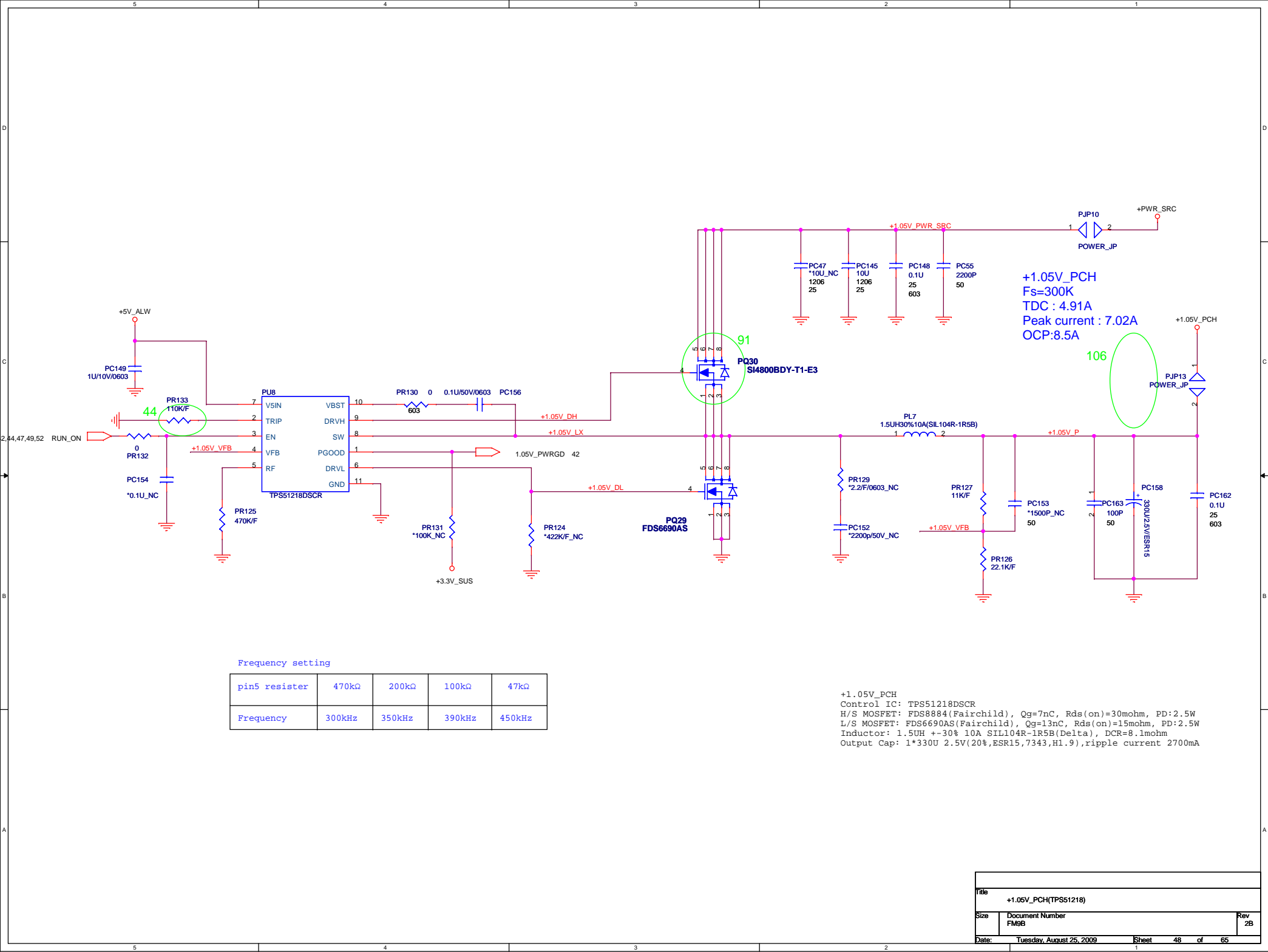
MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	2.5V	VDDQSNS/2	DDR
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)



+1.05V\_PCH  
Fs=300K  
TDC : 4.91A  
Peak current : 7.02A  
OCP:8.5A

Frequency setting

pin5 resistor	470kΩ	200kΩ	100kΩ	47kΩ
Frequency	300kHz	350kHz	390kHz	450kHz

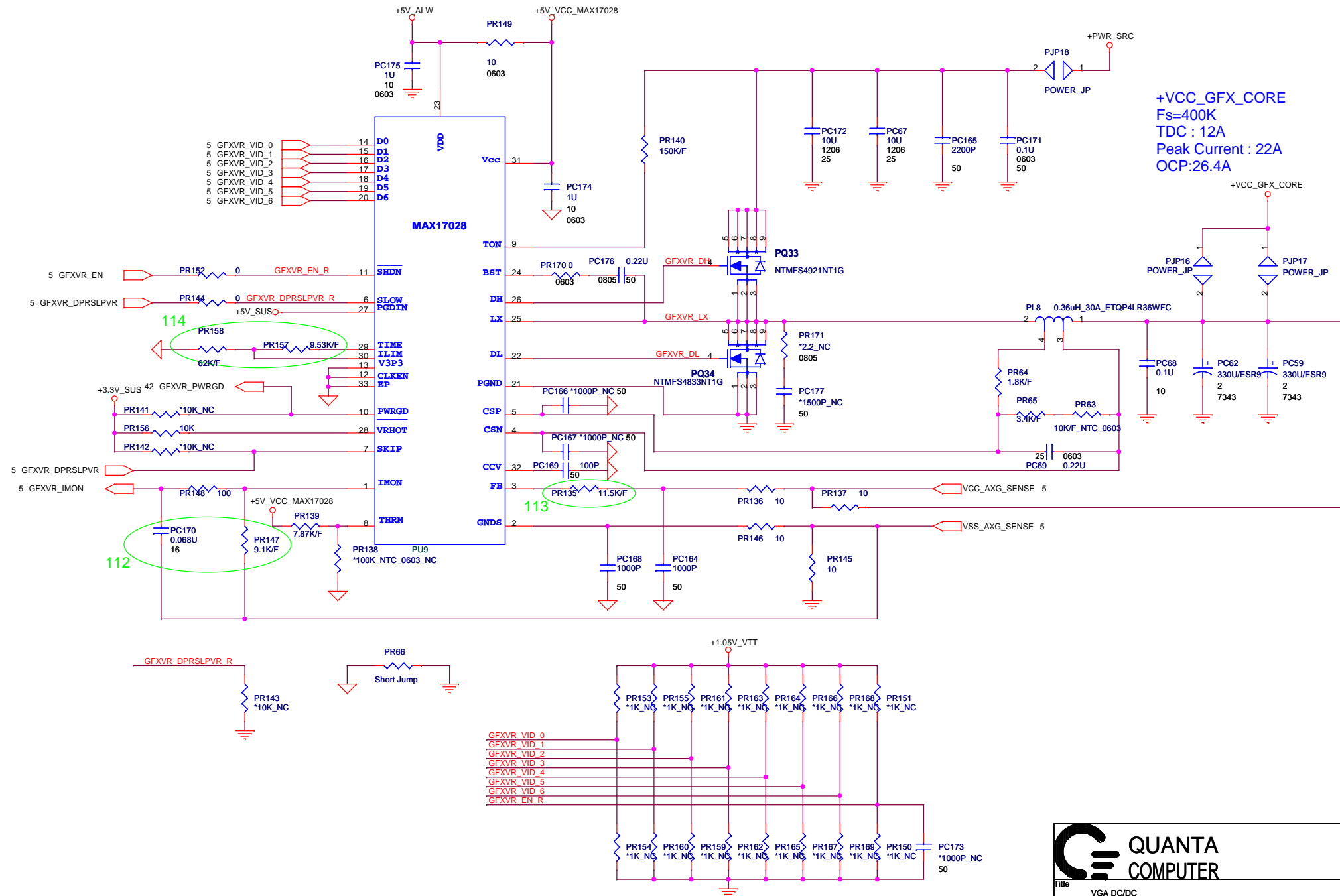
+1.05V\_PCH  
Control IC: TPS51218DSCR  
H/S MOSFET: FDS8884(Fairchild), Qg=7nC, Rds(on)=30mohm, PD:2.5W  
L/S MOSFET: FDS6690AS(Fairchild), Qg=13nC, Rds(on)=15mohm, PD:2.5W  
Inductor: 1.5uH +-30% 10A SIL104R-1R5B(Delta), DCR=8.1mohm  
Output Cap: 1\*330U 2.5V(20%,ESR15,7343,H1.9),ripple current 2700mA

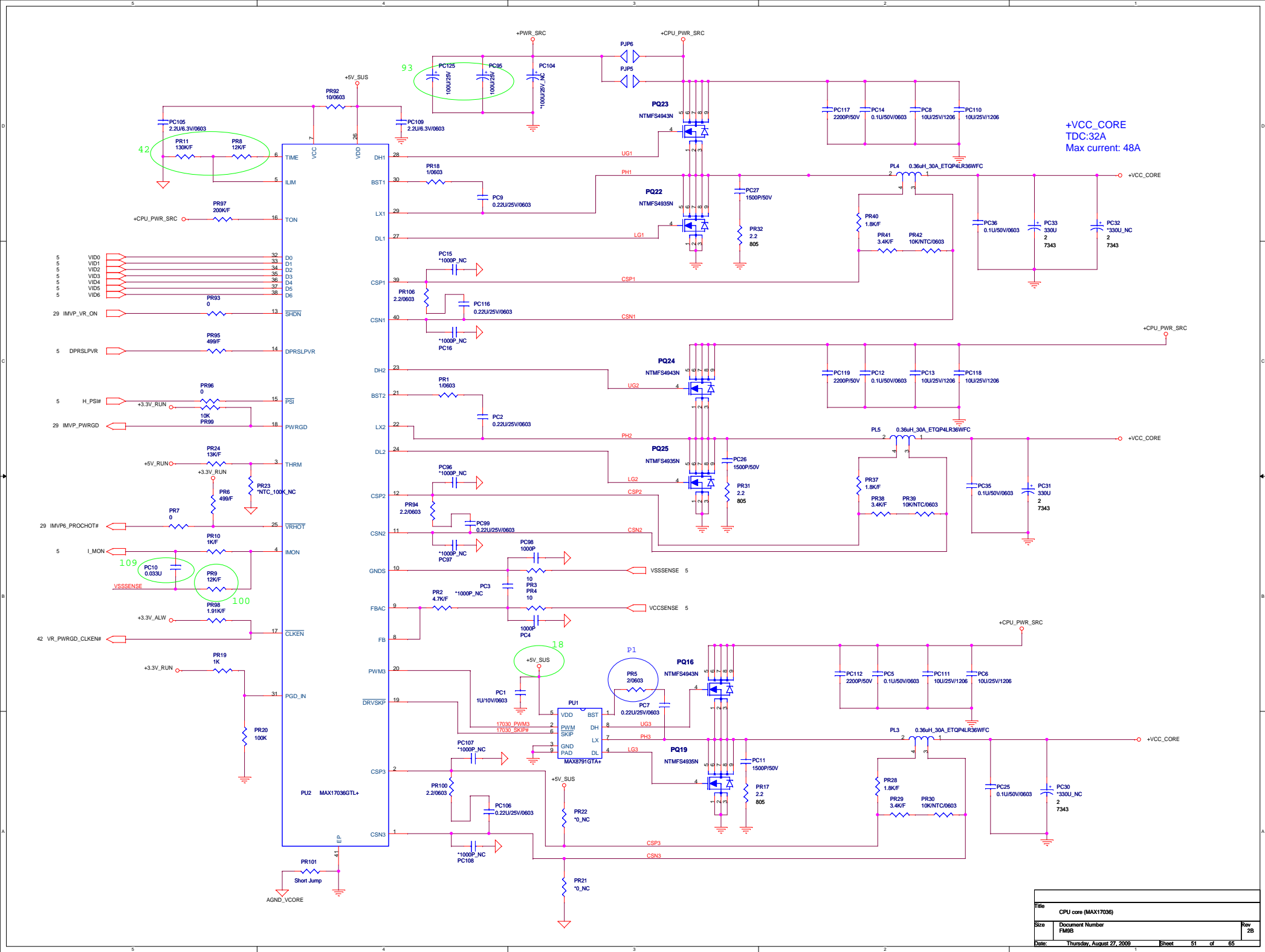


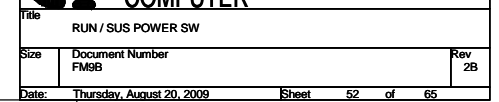
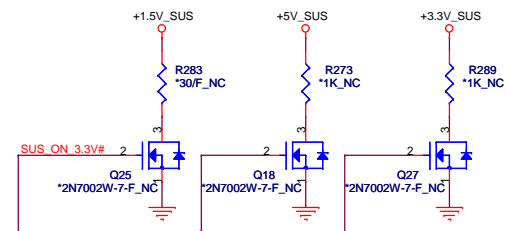
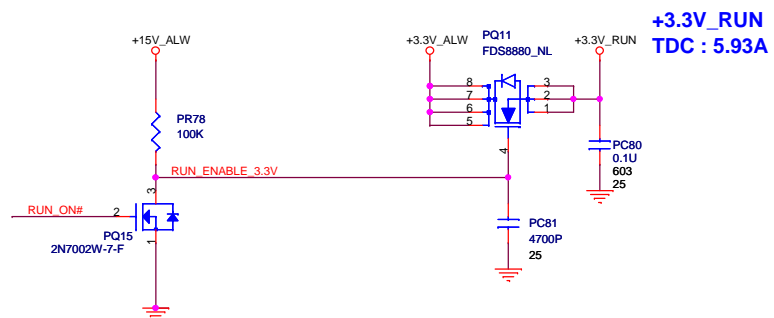
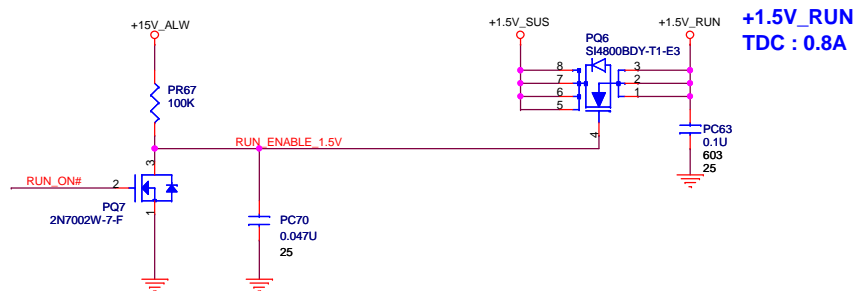
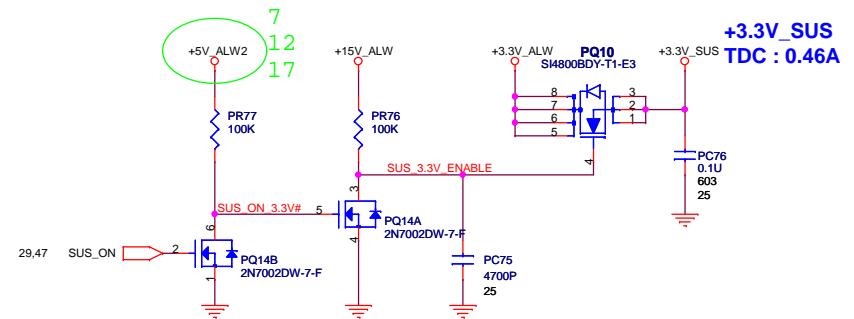
pin5 resistor	470k $\Omega$	200k $\Omega$	100k $\Omega$	47k $\Omega$
Frequency	300kHz	350kHz	390kHz	450kHz

```
+1.1V_VTT
Control IC: TPS51218/DS90CD03
H/S MOSFET: FDM8962(Fairchild), Qg=11nC, Rds(on)=14mohm, PD=2.5W
L/S MOSFET: FDM8760(Fairchild), Qg=24nC, Rds(on)=5mohm, PD=2.5W
Inductor: 0.56u +230V 21A(ETQP4LR56WFC)(Panasonic), DCR=1.6mohm
Output Cap: 2*330u 2V(-10%,-35%,7343,ESR=9), ripple current 3000mA
```

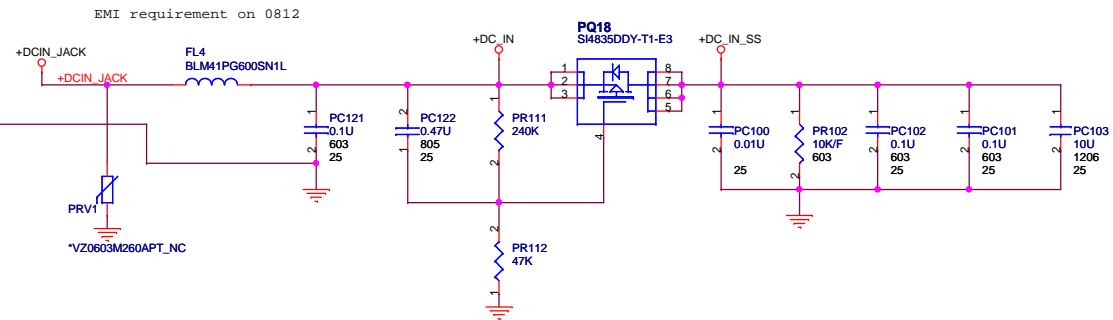
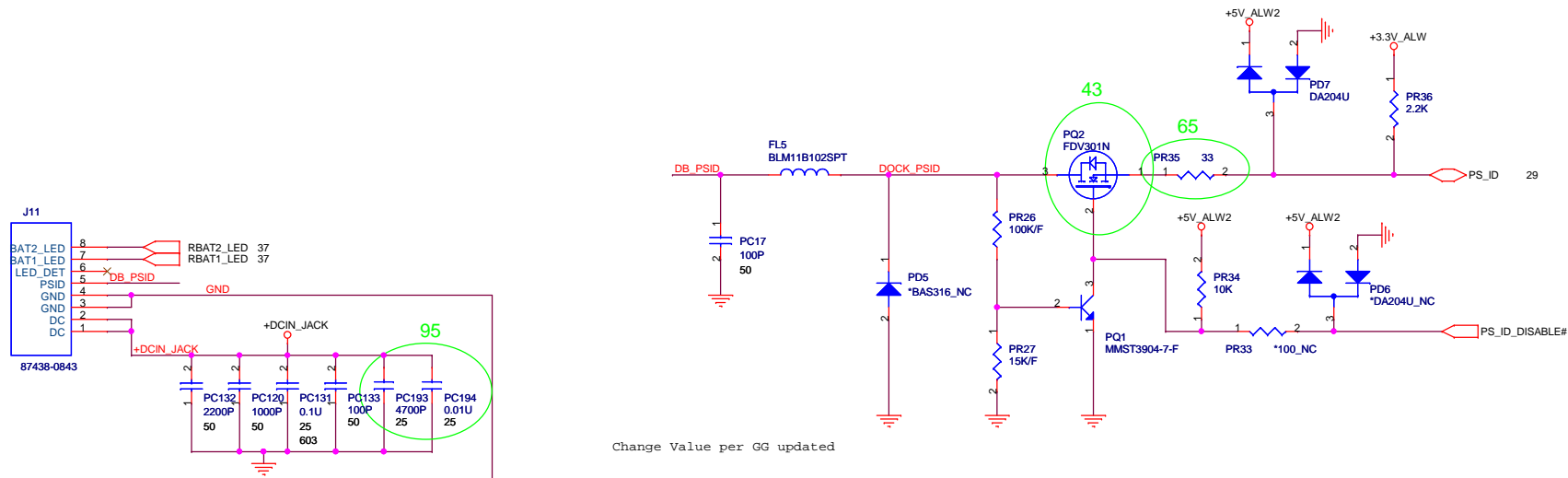
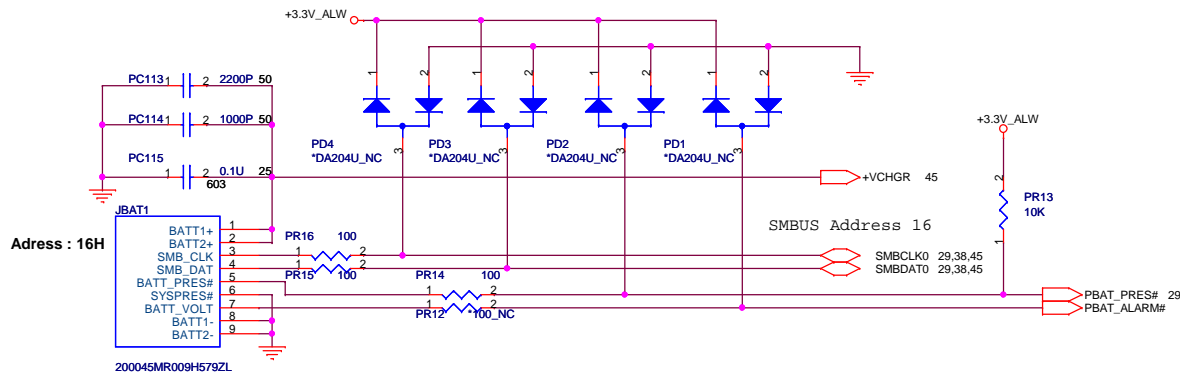
Title			
+1.05V_VTT(TPSS1218)			
Size	Document Number		Rev
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Title  
DCIN,BATT CONNECTOR

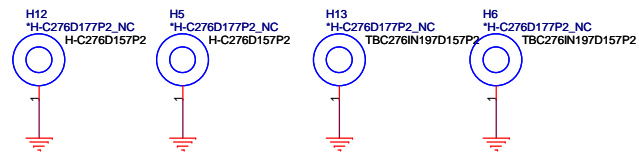
Size  
Document Number  
FM9B

Rev  
2B

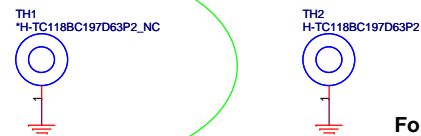
Date: Thursday, August 20, 2009

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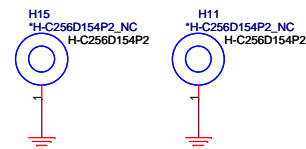
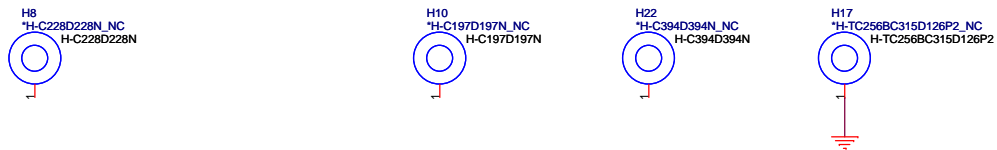
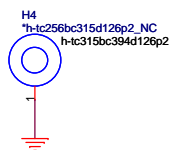
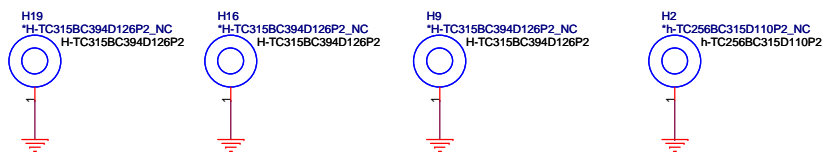
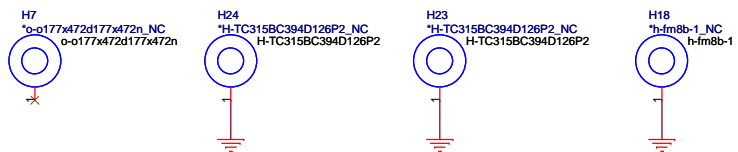
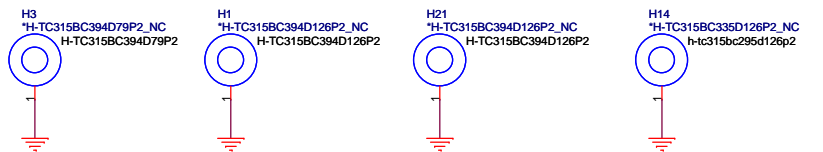
# FOR CPU use



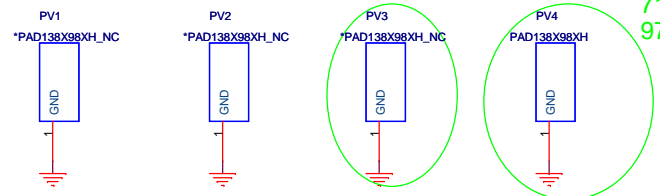
87



For MiniCard nut use.  
on 31' header



For PCH nut use.




47

71  
97



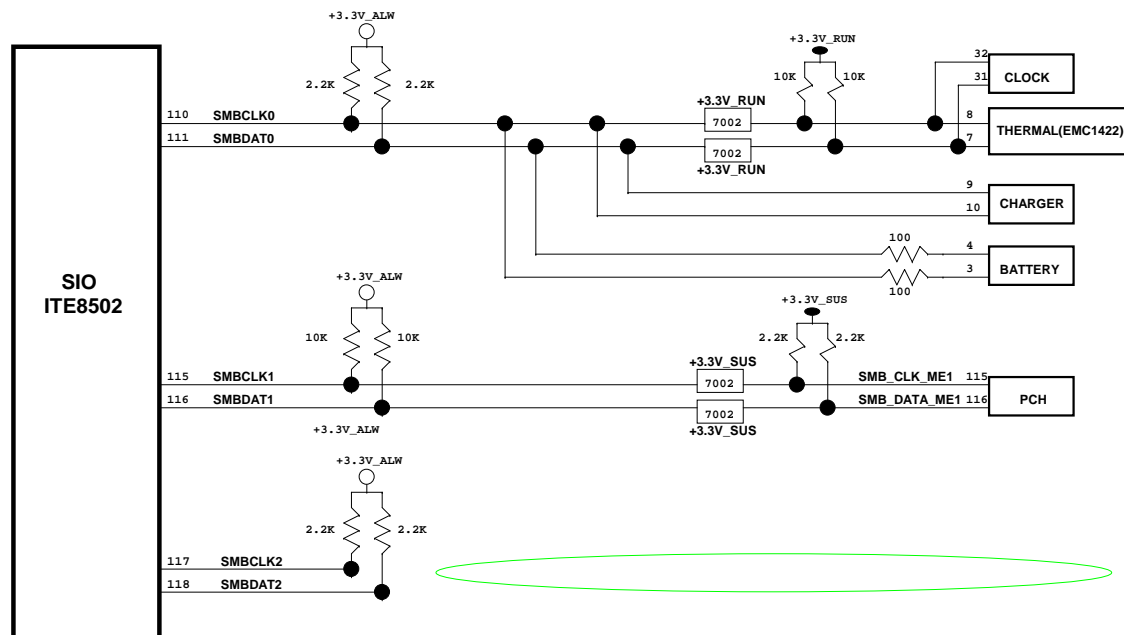
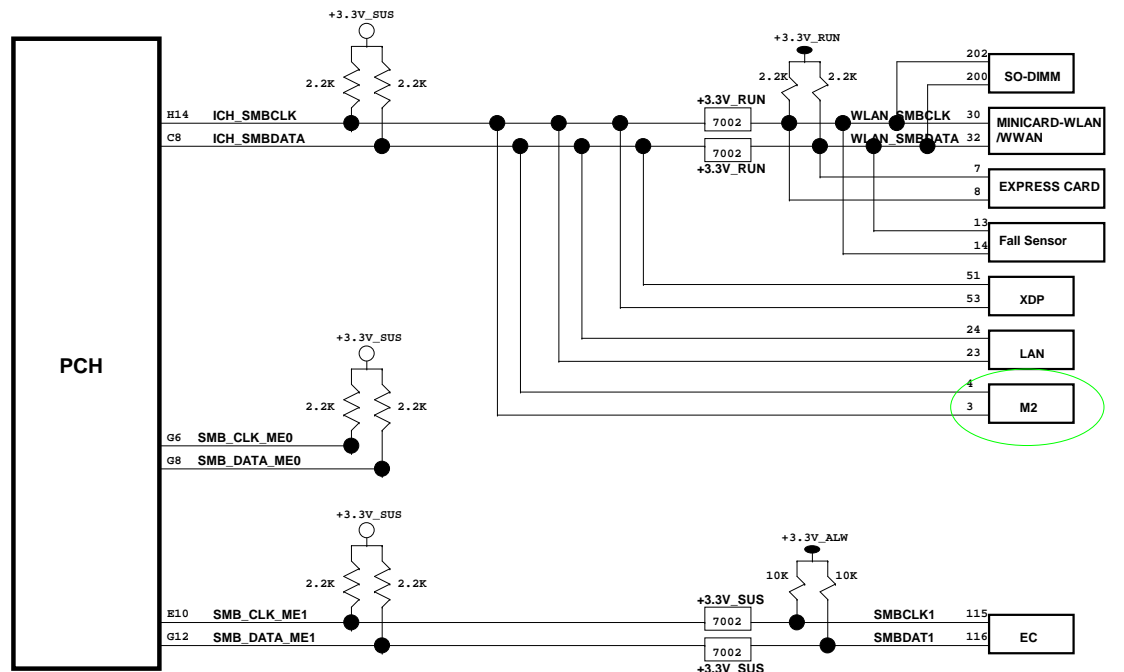
Title			SCREW PAD
Size	Document Number	Rev	
	FM9B	2B	
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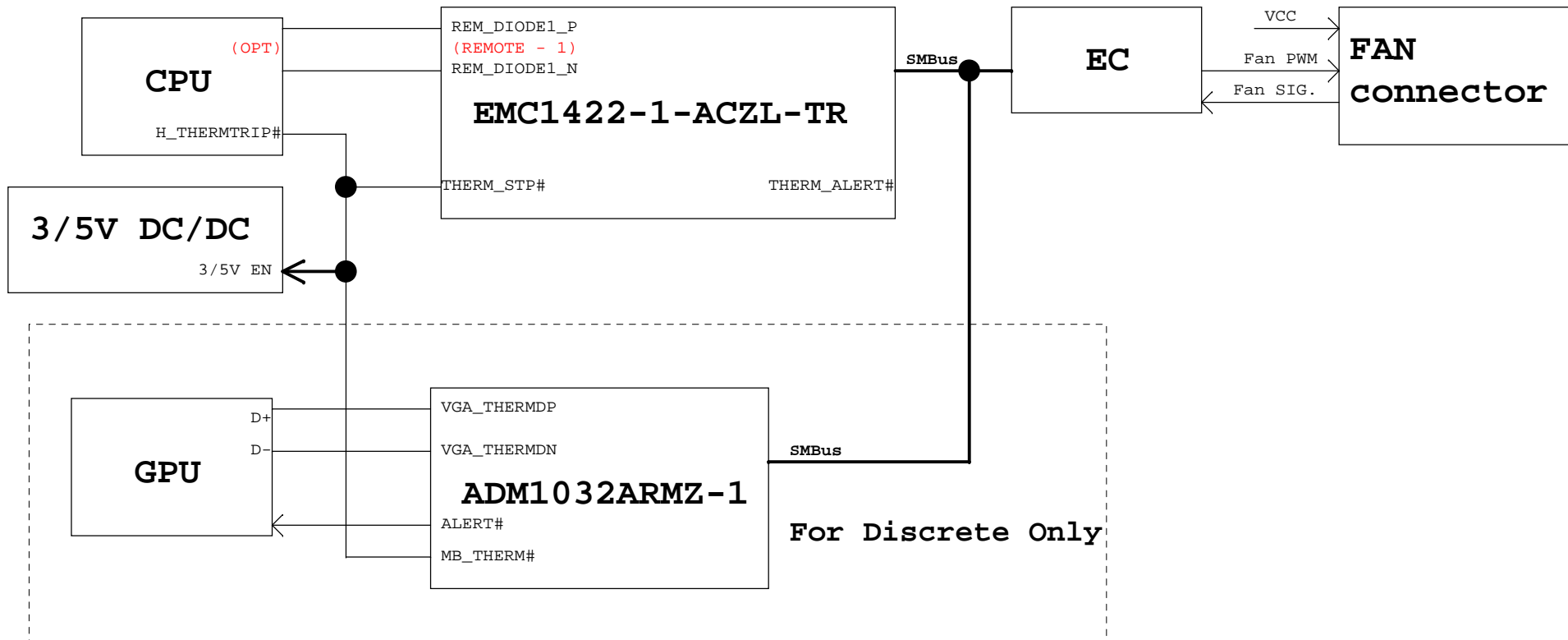
Reserved for EMI.

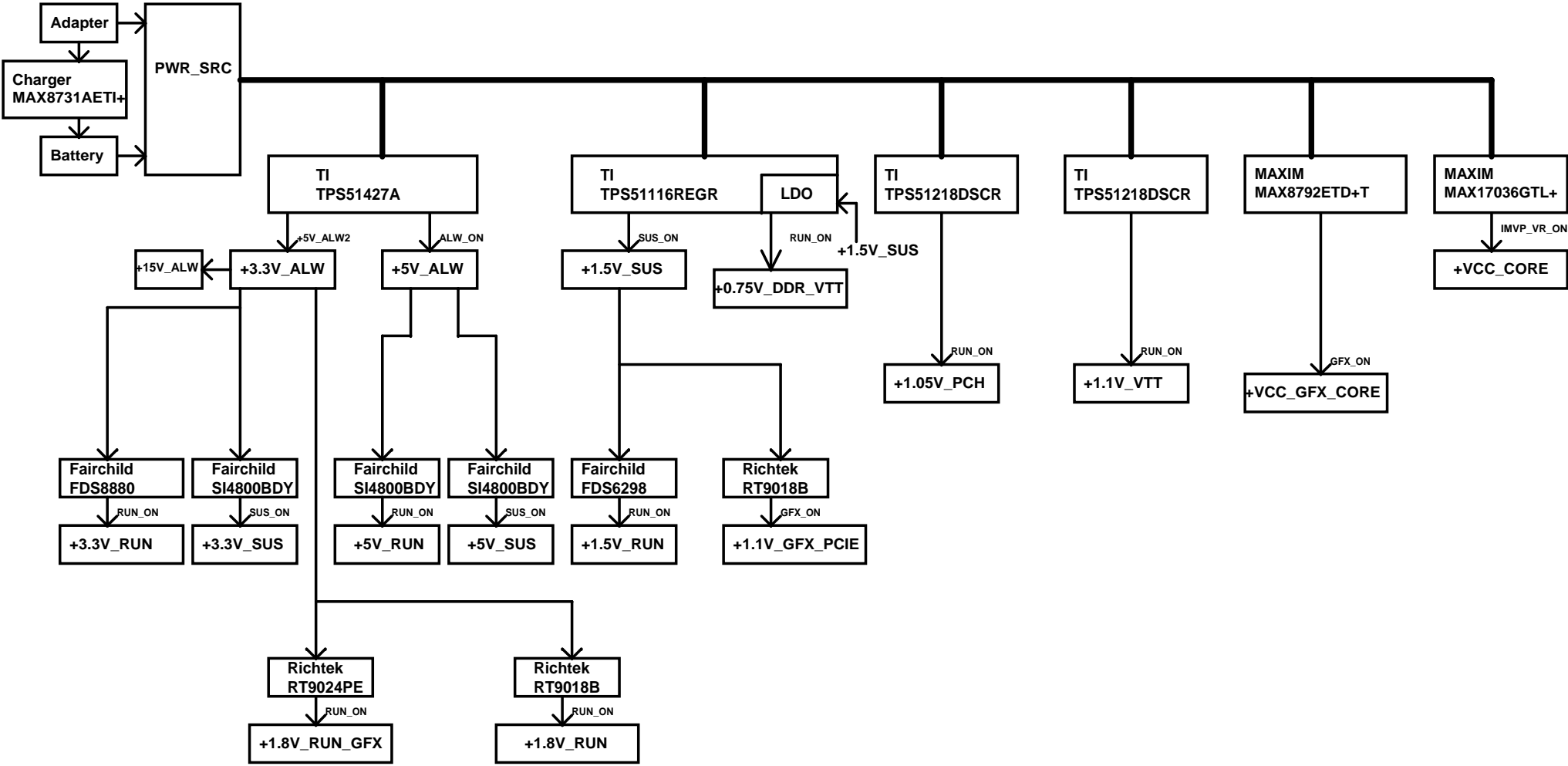


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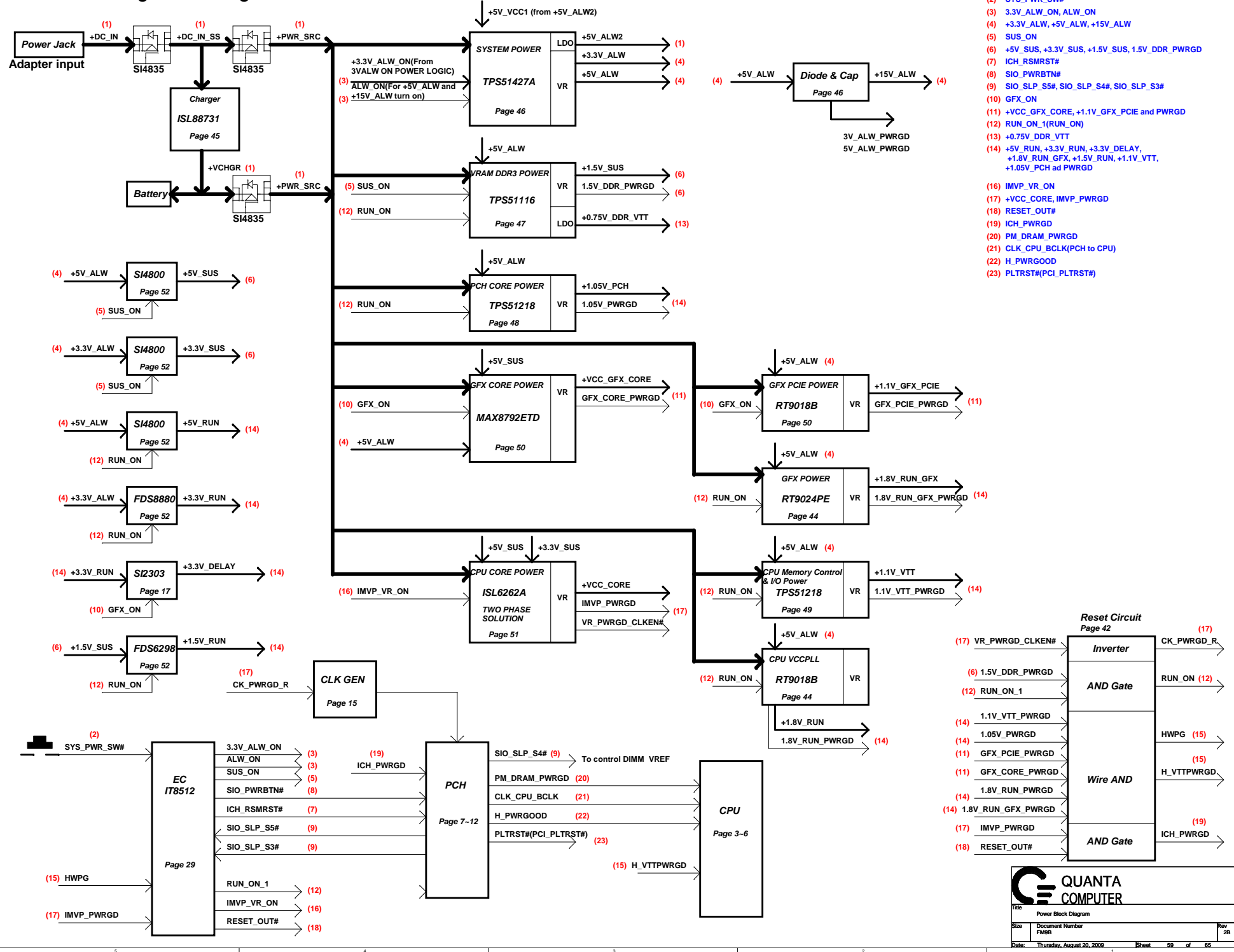
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Size	Document Number	Rev
FM9B		2B
Date:	Thursday, August 20, 2009	Sheet 55 of 65

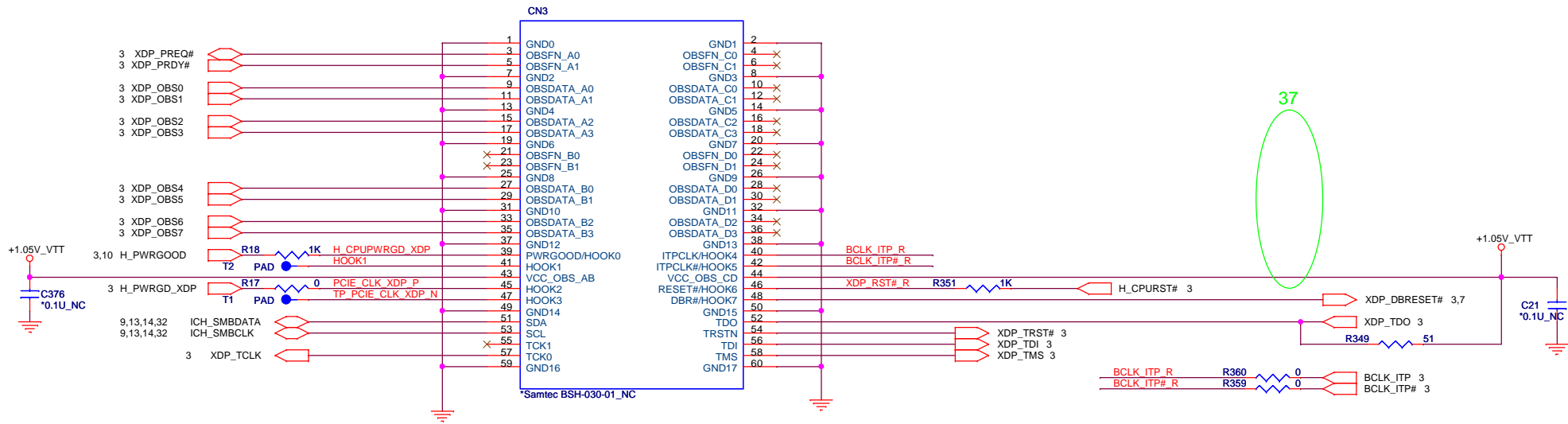







# FM9 Power Design Block Diagram 2009/02/25





It is for debug. requesst vendeer provide 200 pcs sample.

QUANTA  
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Title SMBUS BLOCK		
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